Overview of Digital Integrated Circuit Design I

Course Objectives

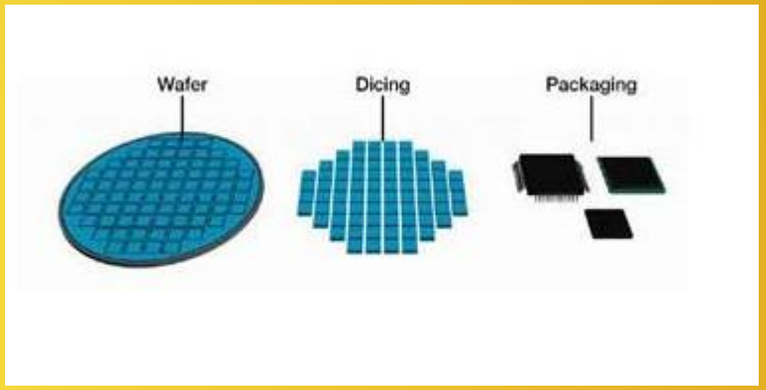
- *Fabless* Digital IC Design
- Design/Layout/Verification of Hand-Crafted Transistors (e.g. Primitive Cell Library)
- Design/Layout/Verification of Functional Circuits Realized with Primitive Cells
- Synthesis of Complex Digital Systems Based on this Hierarchy
- Efficient use of CAD Tools Hosted in Linux
- End Product: *MPW Submission*: *GDS file(s)* → *Pure Play Foundry*
- Design/Project Based Course

- Course Sequence:

ELE 447/448 Digital IC Design I
ELE 537 Digital IC Design II (prereq: 447/448)
ELE 539 Analog IC Design (prereq: 447/448)

Semiconductor Foundries

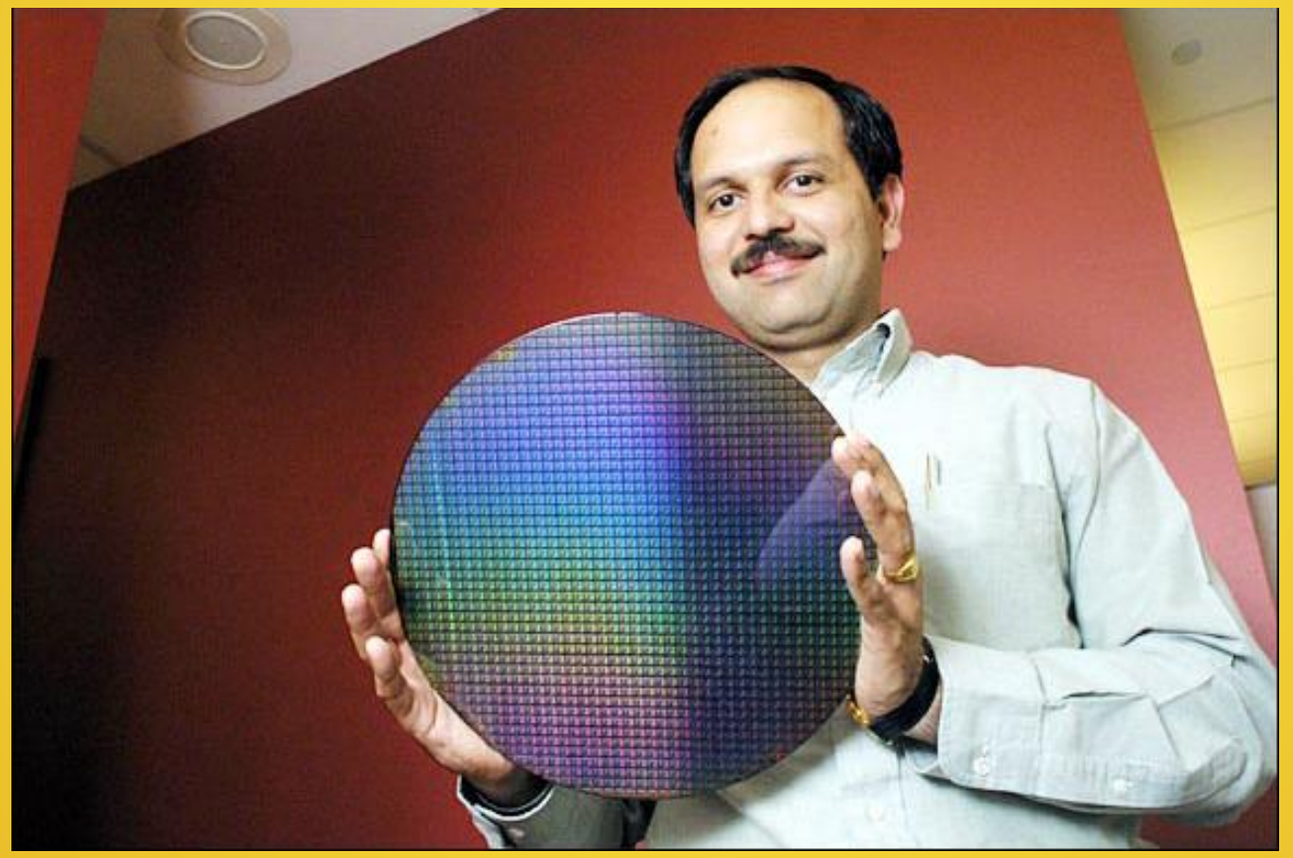
- **Foundry Products: Processed Wafers !!! Reticle Masks are key to wafer processing (Foundry: Masks → Wafer Lots)**
- **Designer Produces a Layout (Mask Geometries) for die; Mask Shop Stitches die Layouts → Reticle Mask**
- A 'chip' is usually a packaged die: 'Chip 2 Product': Wafers → die are cut from wafers → die are then packaged
- 2 Major Business Models: Integrated Device Manufacturer (IDM) & Pure Play
  - Volume Business Regardless of the Business Model
  - Economics drive the development & longevity
  - Huge Capital Investments are Required: $10 Billion or more, in some cases
  - Global Business: Tools & Contracted Services



- IDM: A foundry that fabricates internally developed designs
  - Vertically Integrated from Designers to the Fabrication Lines; Designs are controlled by Foundry Employees ONLY
  - Internally Developed CAD Tools(at least some); Customization & Foundry Integration are 'tight'
  - IDMs sell 'packaged chips'; IDM Customers Buy the 'chips' it manufactures
  - IDM Examples: Intel Corp., Samsung, TI

- Pure Play (or Merchant) Foundry: A foundry that fabricates designs for others
  - Products are the use of the fabrication process & knowledge of the best methods
  - Pure Play Foundries Sell Wafers; Customers buy Wafers (containing the customer's designs)
  - CAD design interface must be distributed to customers→ Infrastructure Required to Distribute Foundry Access
  - Customers dice wafers, then package & sell 'chips' manufactured by the Pure Play Foundry
  - Earliest Formal Example of a Pure Play 'Ecosystem': The MOSIS Service (1980; DARPA)
  - Pure Play Examples: Taiwan Semiconductor Corp (TSMC), Global Foundries (GF), Tower Semiconductor

Typical CMOS Foundry Wafers are 200mm & 300mm:
IBM 300 mm Wafer



Pure Play Foundry Model

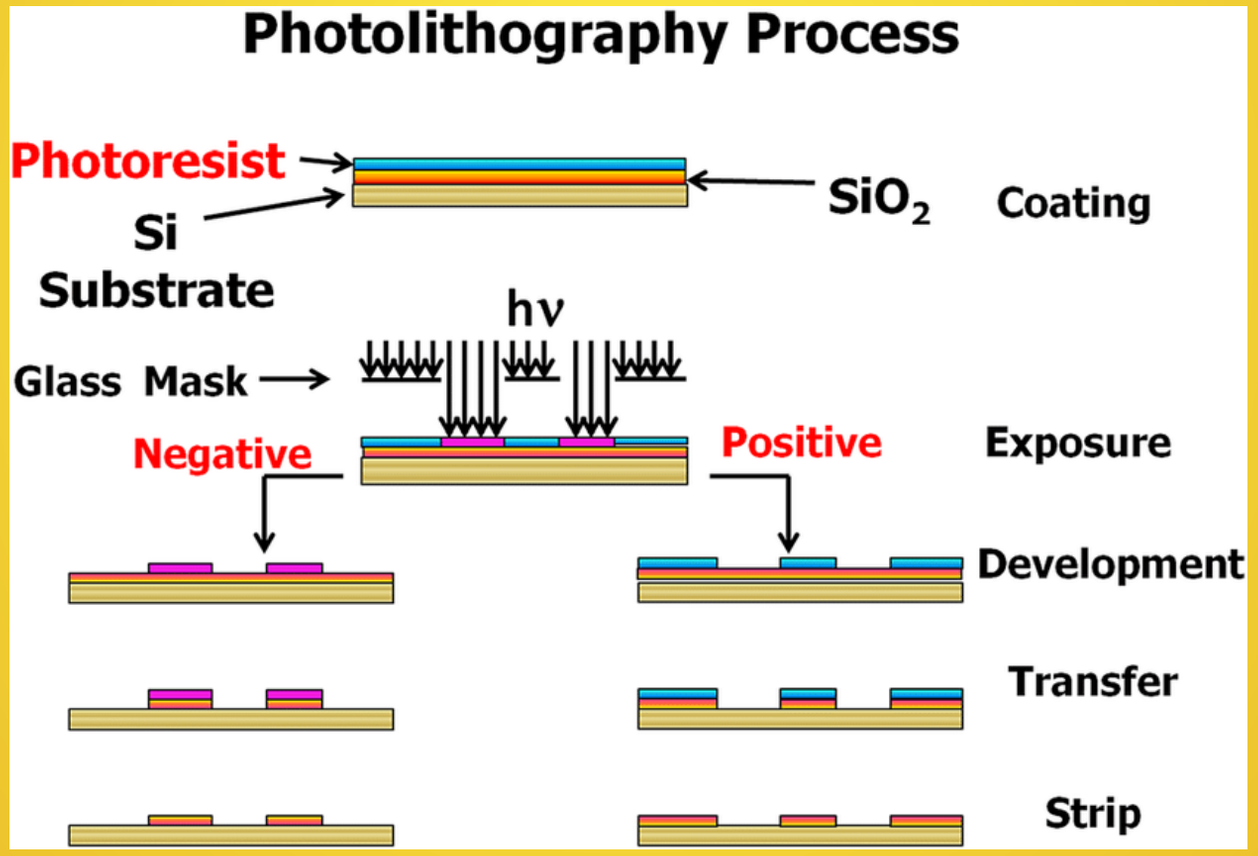
- Pure Play Customers: Fabless companies, device mfg's, Government labs, universities, even other foundries
  - Capitol investments are minimized; so the customer can be a small business
  - The Customer must have knowledge about the Foundry Process Technology
  - The Customer is making a custom design
- Steps (Enablement: 1 &2):

  1- Non-disclosure agreement (NDA) signed by customer & foundry
  2- Foundry supplies process design kit (PDK) to customer; the PDK is usually DATA
  3- Customer uses PDK to generate a gds file containing layout(s)
  4- Foundry fabricates wafers from gds file supplied by customer(s)
  5- Wafers are delivered to the customer
  6- Wafers are tested and/or diced & tested on a board level
- Rules/Ethical/Legal Considerations
  - The NDA is a Legally Binding Document for both the Foundry & the Customer
  - The PDK is **Intellectual Property** owned by the Foundry & Is **Proprietary** (so, it cannot be 'shared' without the Permission of the Foundry; *even if the party sharing has an NDA !*)
  - The Customer agrees (*in the NDA*) to **Protect the PDK DATA & Documentation**
  - The Foundry agrees (*in the NDA*) to Protect the customer's **Design Submission DATA** (The Foundry goes to great lengths to prevent 'sharing' of customer data)
- Violations of the 'Rules' Can Result in:
  - Fines, Law Suits & other Civil Actions
  - Criminal Charges
  - Severe Damage to a Company's or Individual's Reputation
  - Loss of Customer Base (which the Foundry Needs to exist)

Photolithography → Selection Using Mask

This is done at least 1x for each processing step (1 of 30-100 steps)

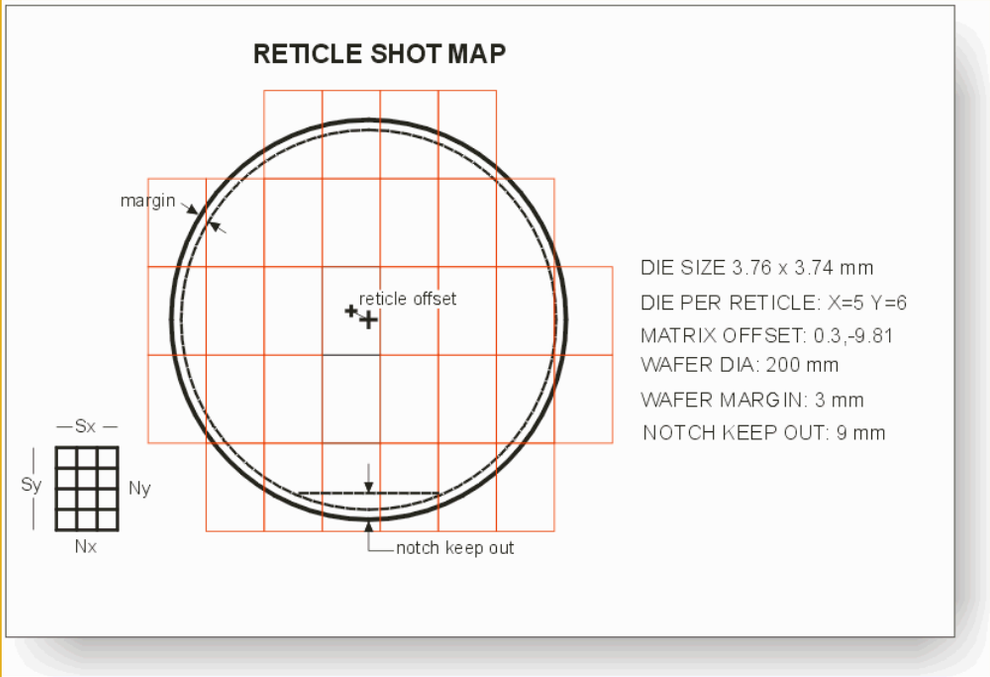
The Layout Contains a Complete Set of Masks for a Particular Design

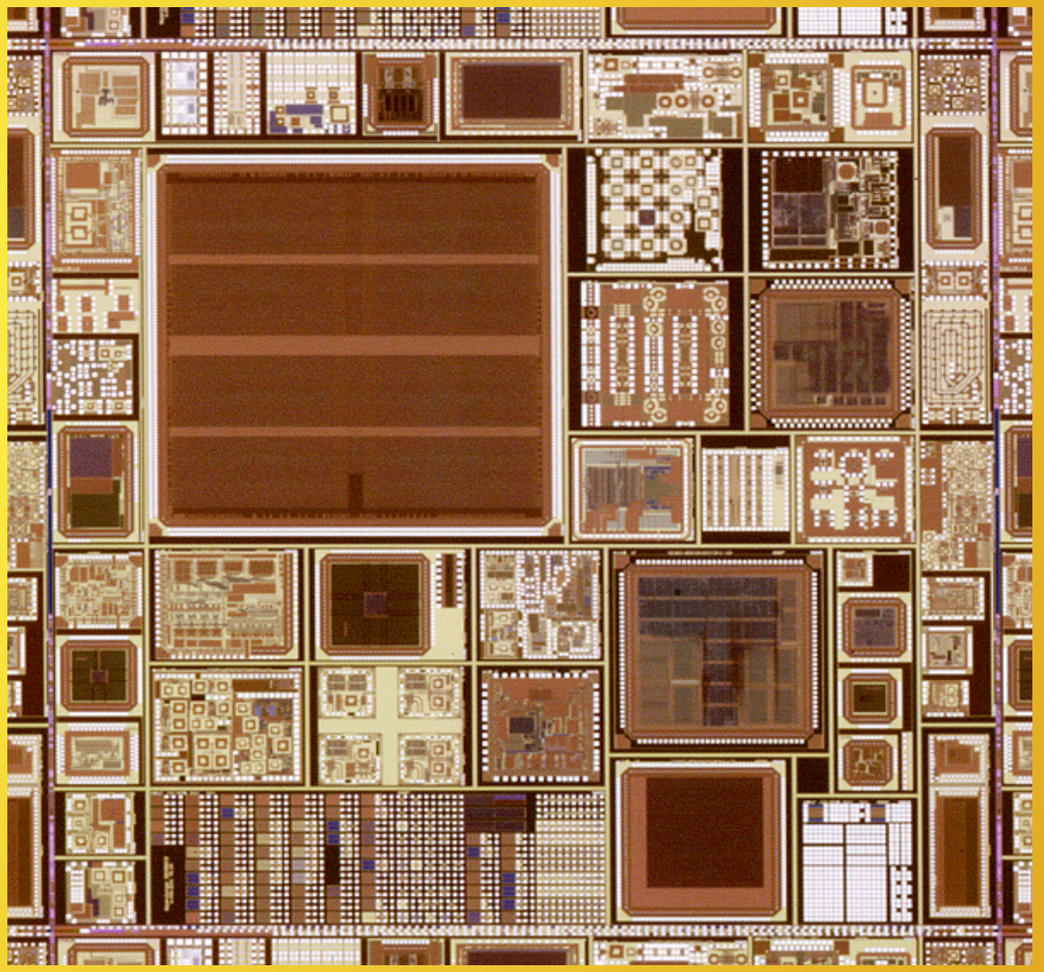


What is in a PDK ?/How is it used ?

- Process Design Kit (PDK) Contents (**PRORIETARY: Intellectual Property of the Foundry !!!**)
  - SPICE Circuit Models of key devices
  - Technology files
  - ALL Mask Layers (pseudo & real)
  - Design Rules for the Mask Layers
  - Rules for Layout vs. Schematic (LVS)
  - Design Manual & other documentation
  - ESD Guidance
  - Test results from wafers & devices
- PDK is integrated into the CAD Tool
  - PDK Data is integrated into the CAD Tool software (by the user)
  - CAD Tool environment will adapt & morph into the PDK's environment
  - ONLY CAD Tools supported by the foundry can use the PDK
- PDK functions
  - Simulation of Circuit Design
  - Layout Generation
  - Design Verification
  - Generation of GDS files for design submission

What is an MPW & Picture of MPW Reticle





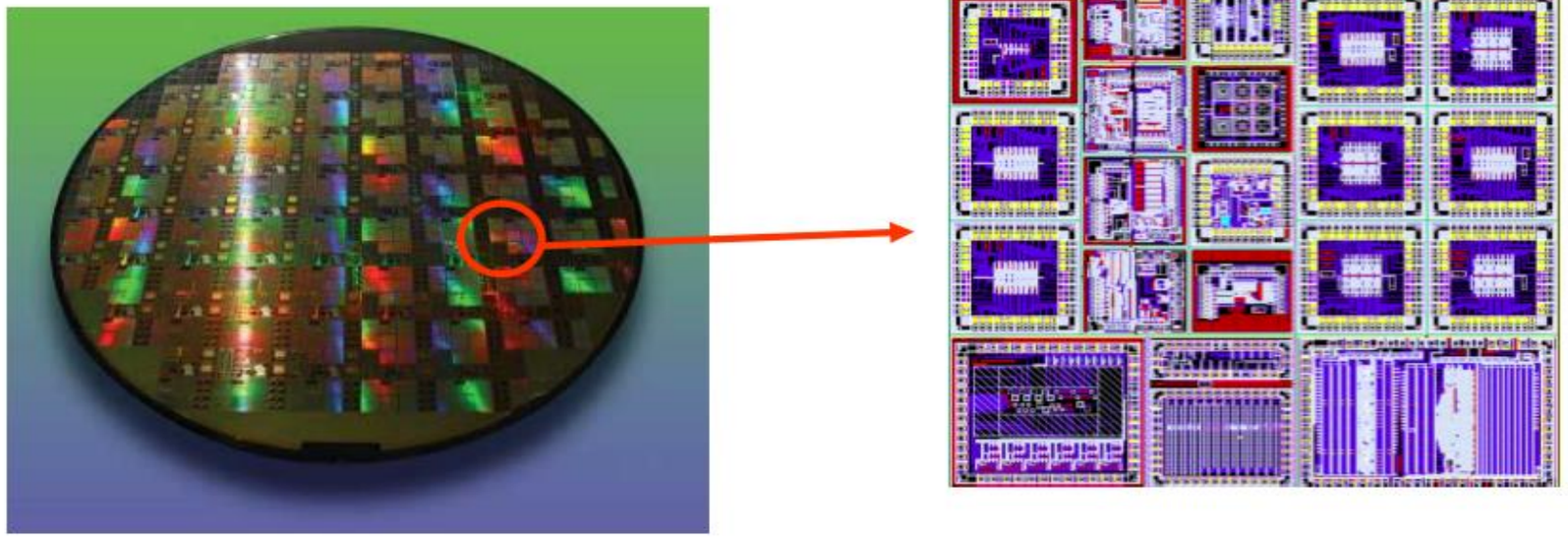
- Pure Play (or Merchant) Foundry: Multi-Project Wafer (MPW)

- Pure Play Foundry Wafers can Contain a Single Dedicated Design or Multiple Customer Designs

- Multi-Project Wafers are a 2nd ‘ary product: Shared cost for prototyping

Multi-Project Wafers

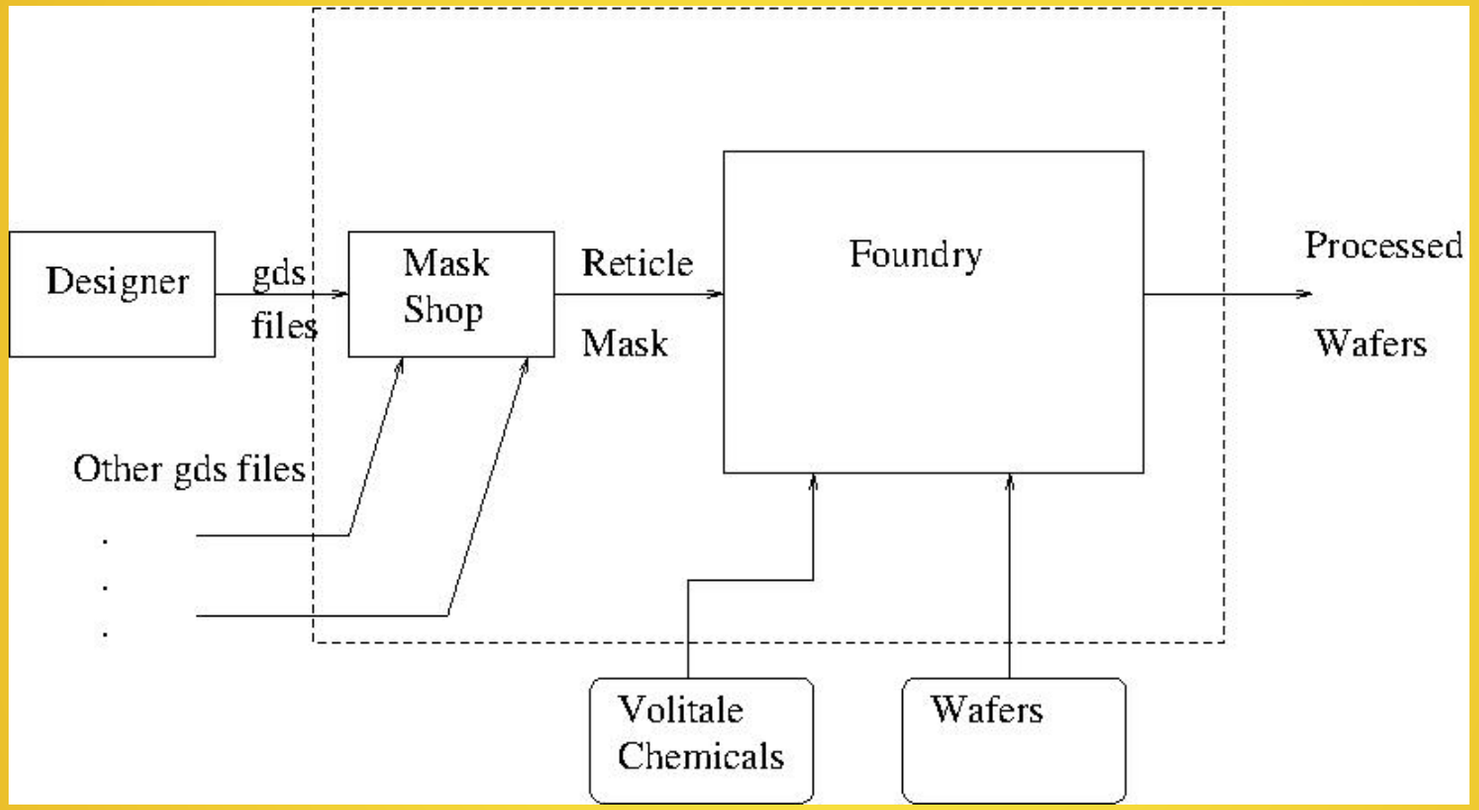
- Mask set cost: >$1M for 90 nm technology
- **Share cost of mask tooling between multiple designs!**
  - Prototyping
  - Low volume production

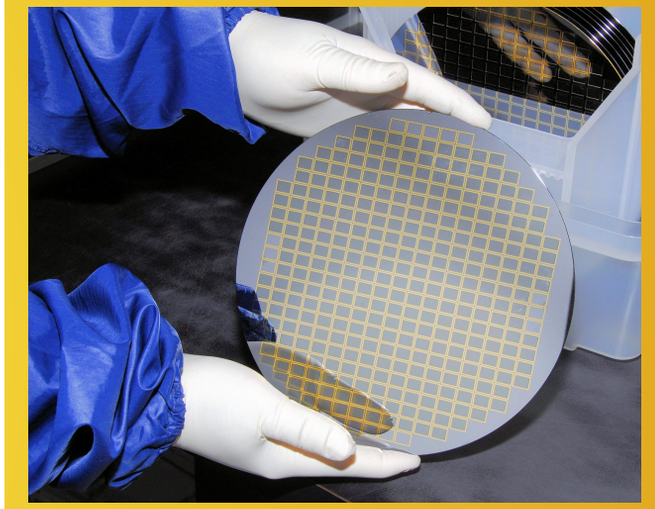


Images courtesy of EuroPractice and CMP

Summary of Wafer Fabrication Process

Dedicated Wafer run would repeat the same die layout from a single gds file; An MPW would integrate multiple die layouts contained in multiple gds files from different designers

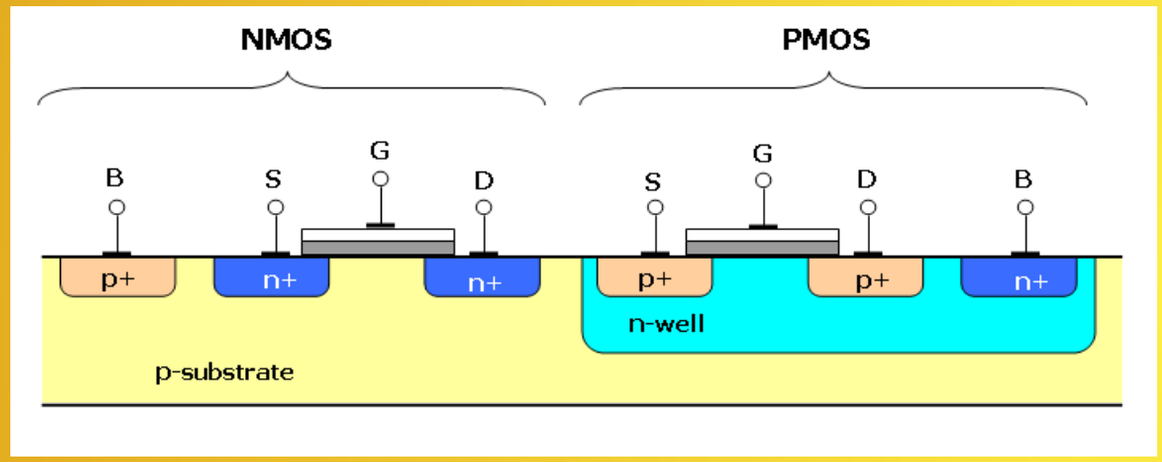




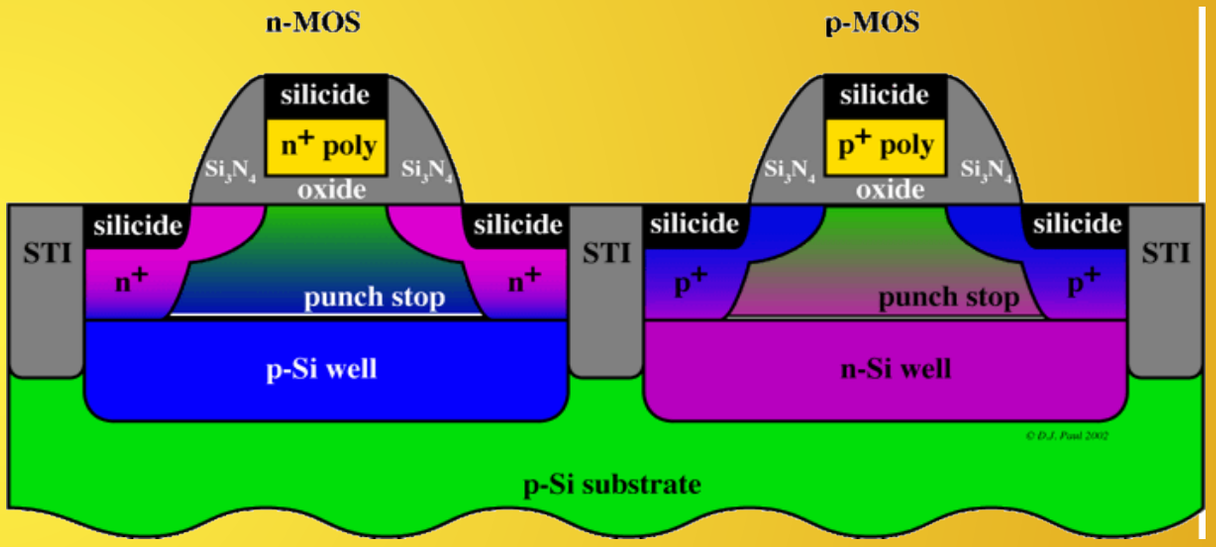
More volatile chemicals than used by both of these characters combined

Blank/pre-doped wafers are supplied by vendor(s)

Bulk CMOS Cross Sections



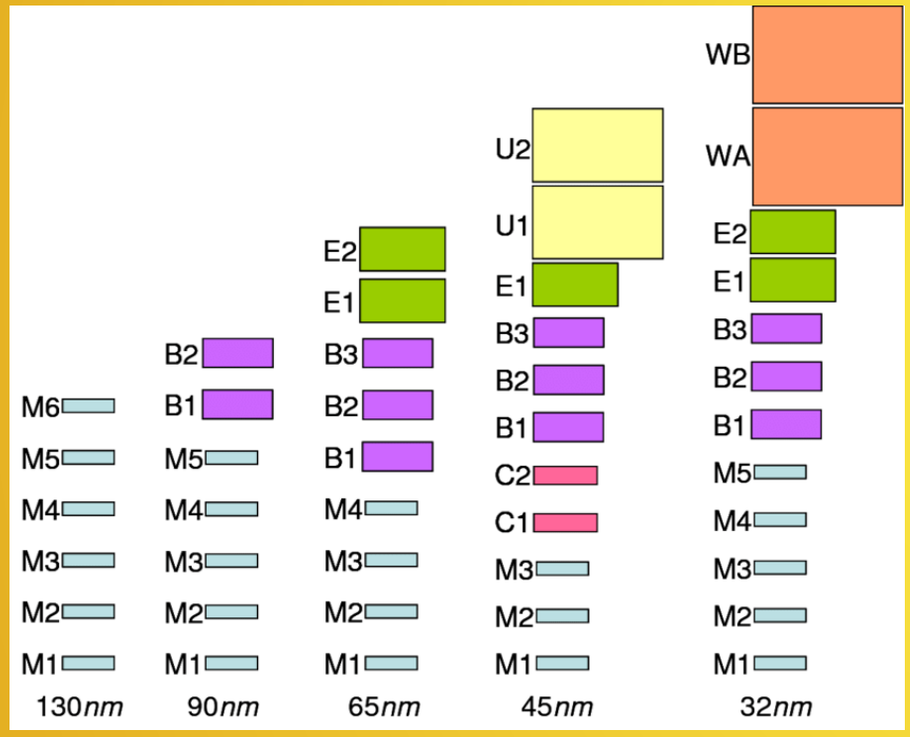
Simple



Detailed (no Body Contact Shown)

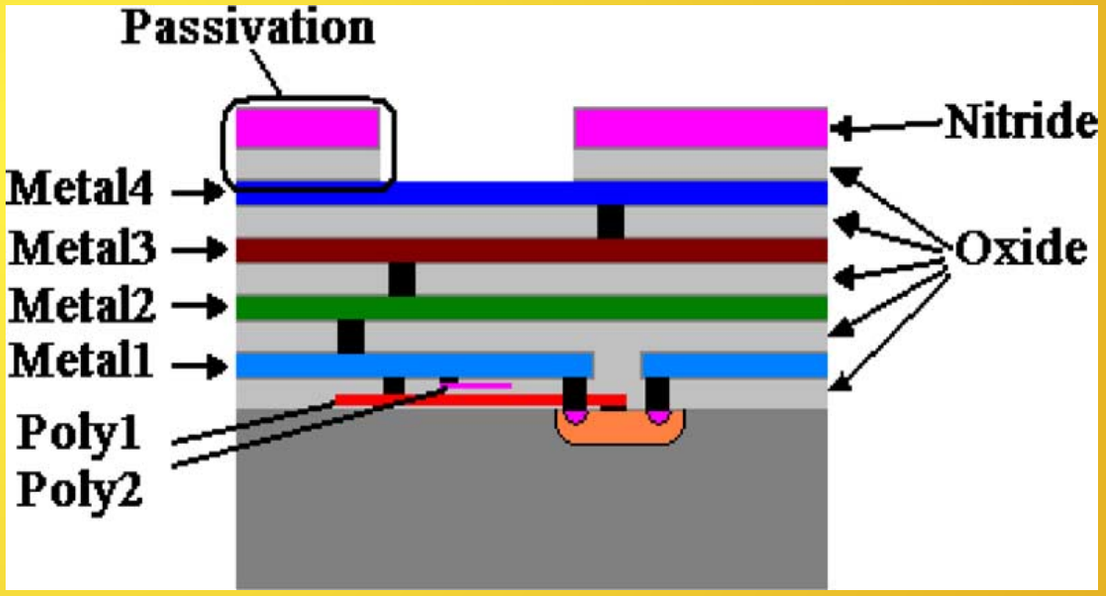
Metal Stacks

(Processes Often Provide Several Metal Stack Options)



Metal Stacks for 130nm thru 32 nm

(caps, resistors & inductors can be implemented)



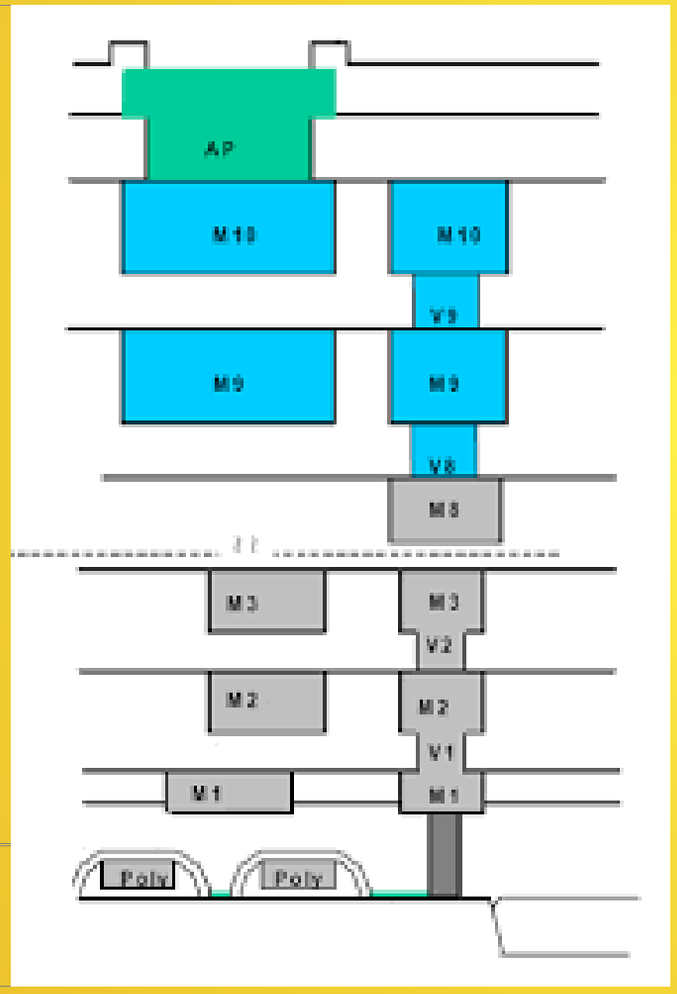
Example of Metal Stack with 2 Poly Layers

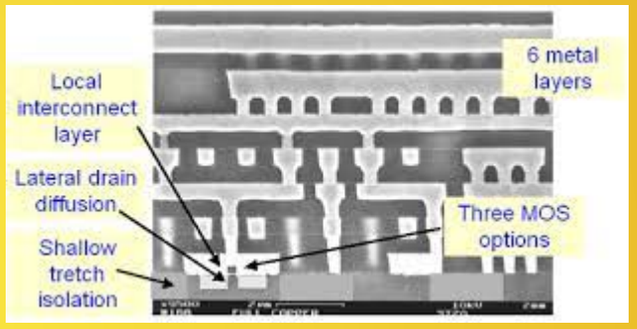
Caps can be realized with 2 poly layers

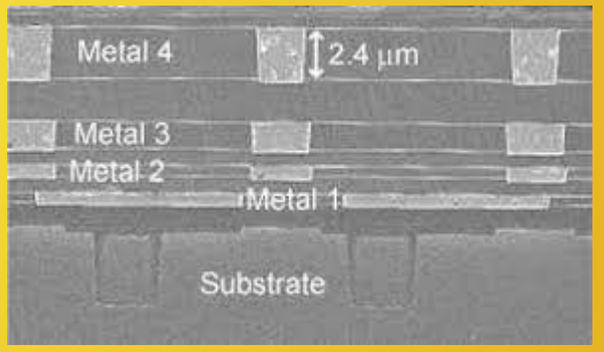
180nm SiGe BiCMOS with FEOL & BEOL

BEOL

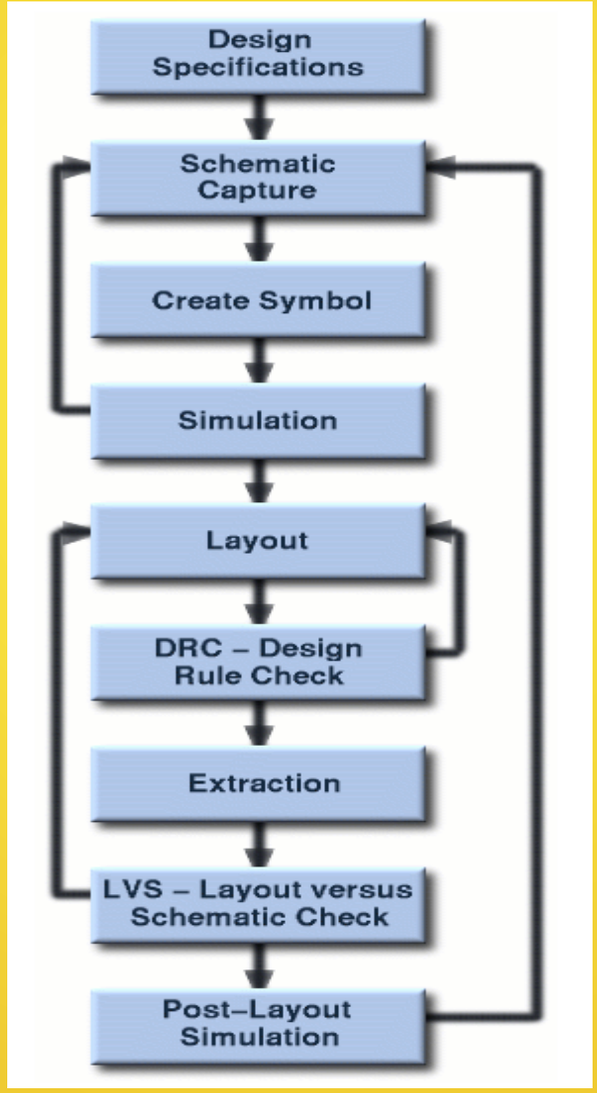
FEOL



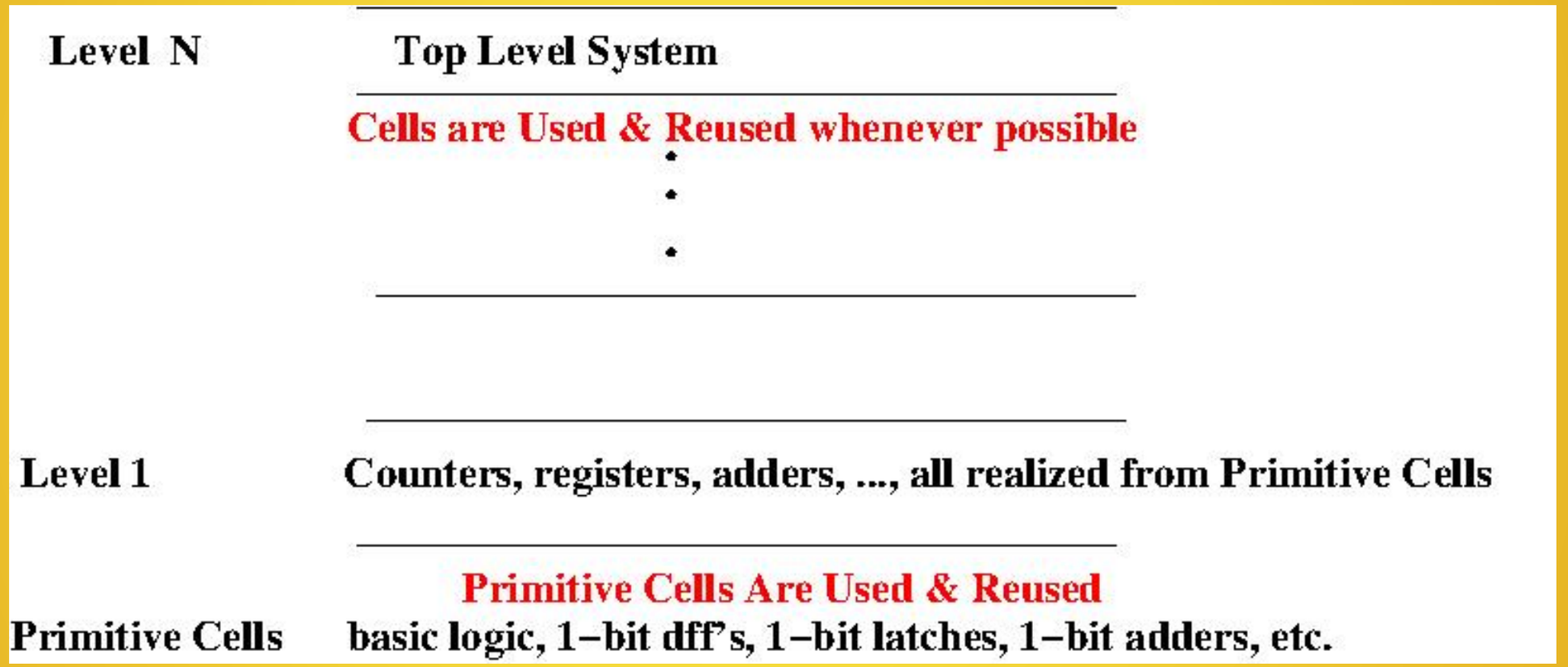




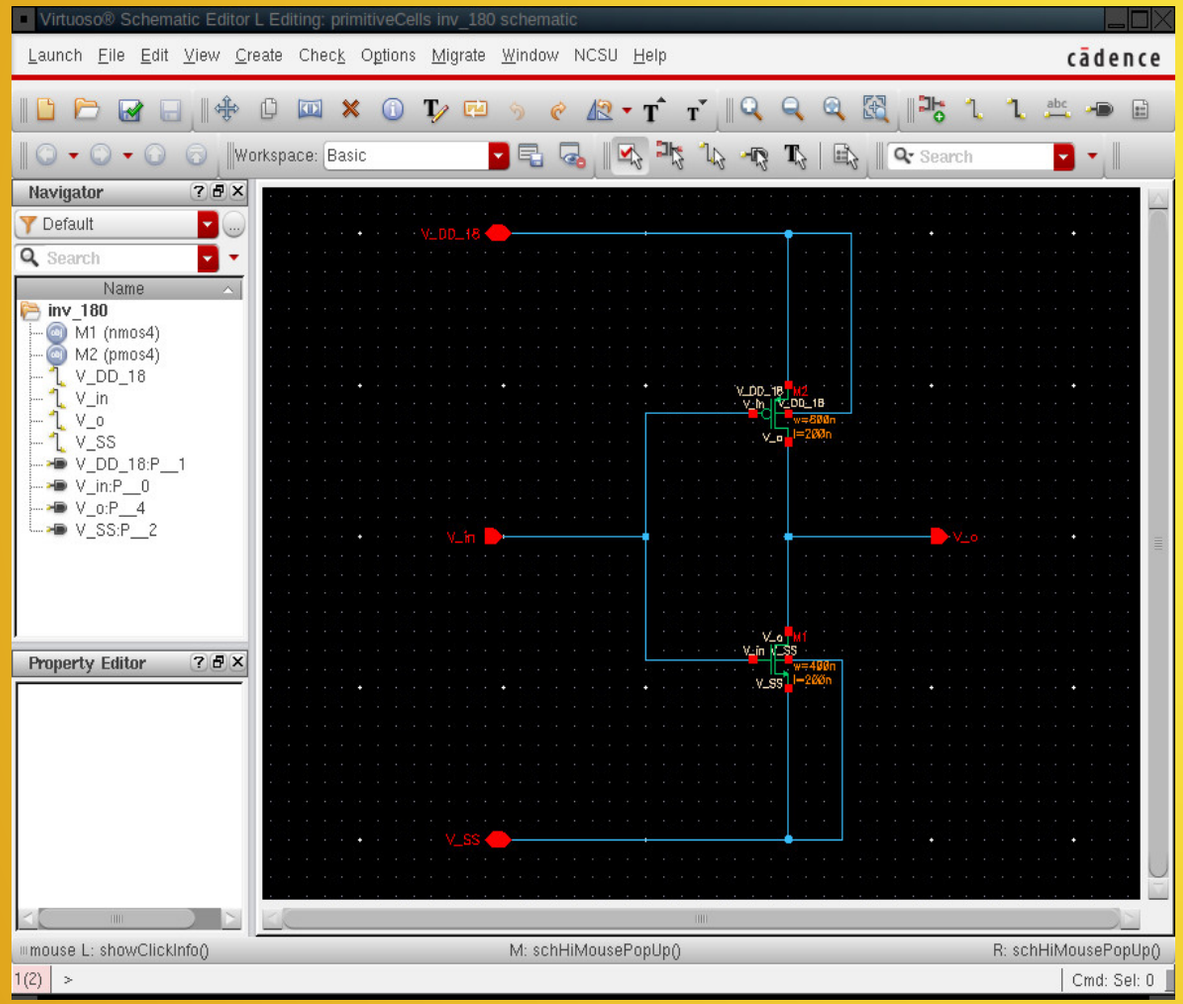
Design Flow

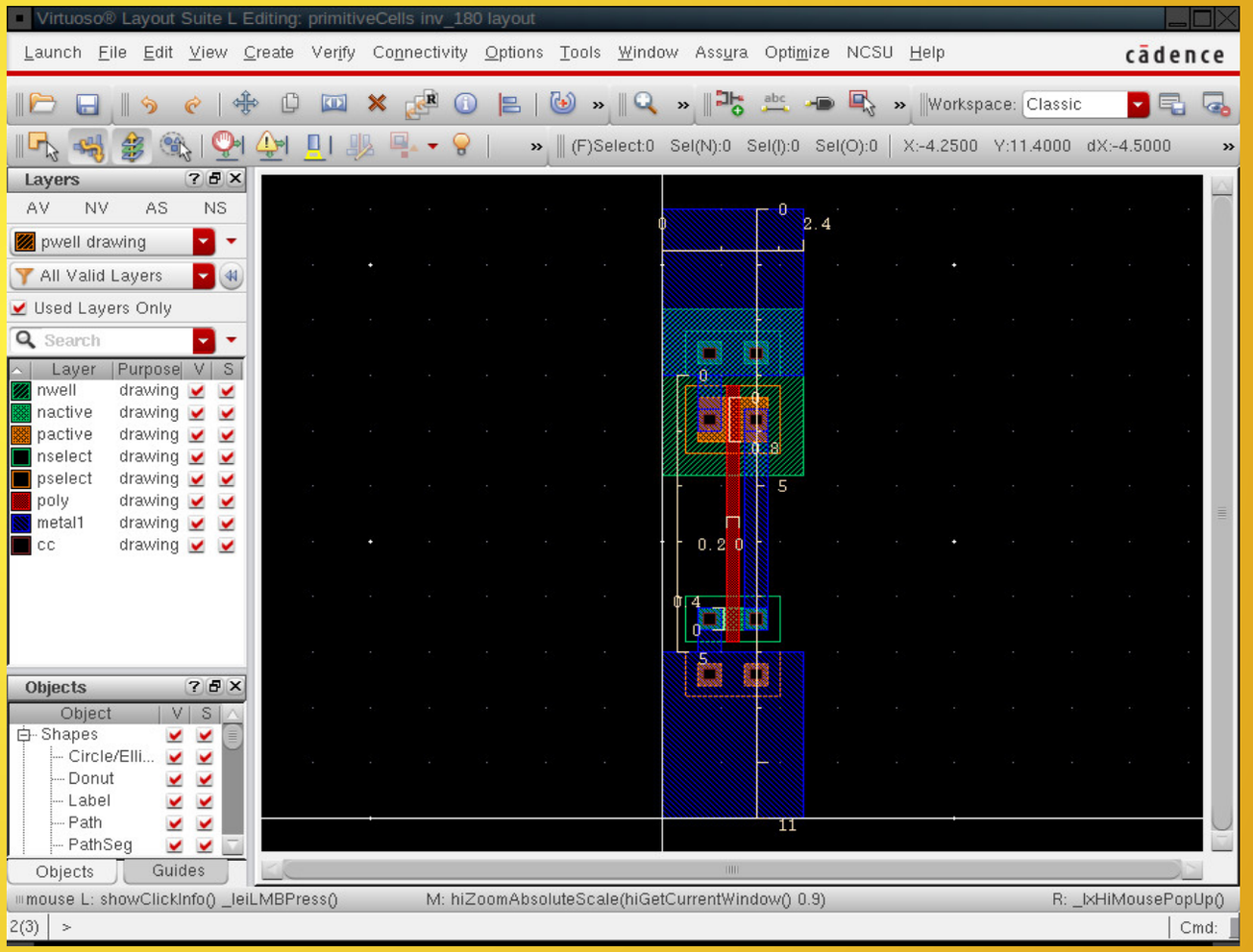

Design Specifications
Schematic Capture
Create Symbol
Simulation
Layout
DRC – Design Rule Check
Extraction
LVS – Layout versus Schematic Check
Post–Layout Simulation

Hierarchy & Reuse

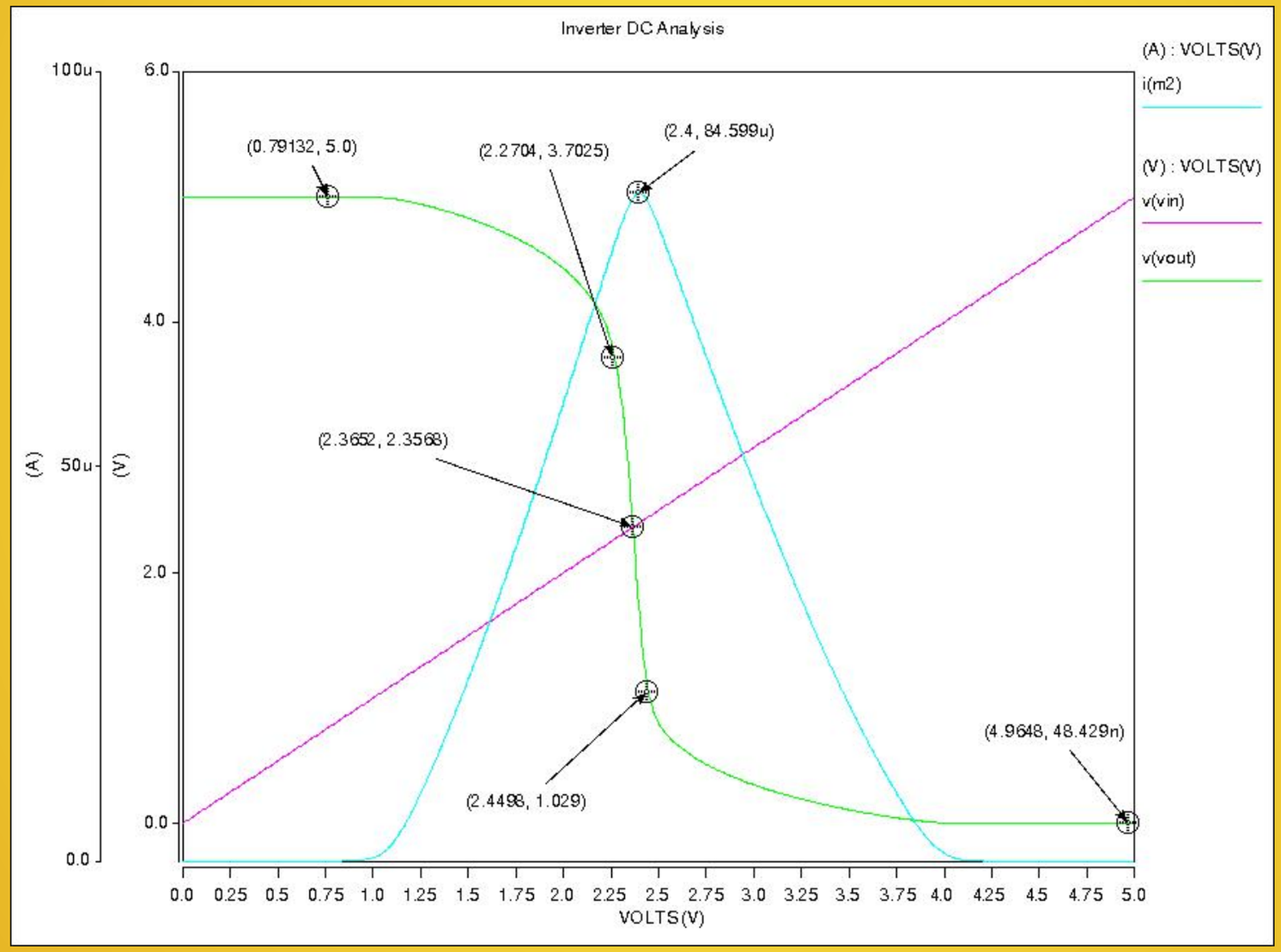


Virtuoso Schematic Editor & Layout Editor Example: Inverter 180nm

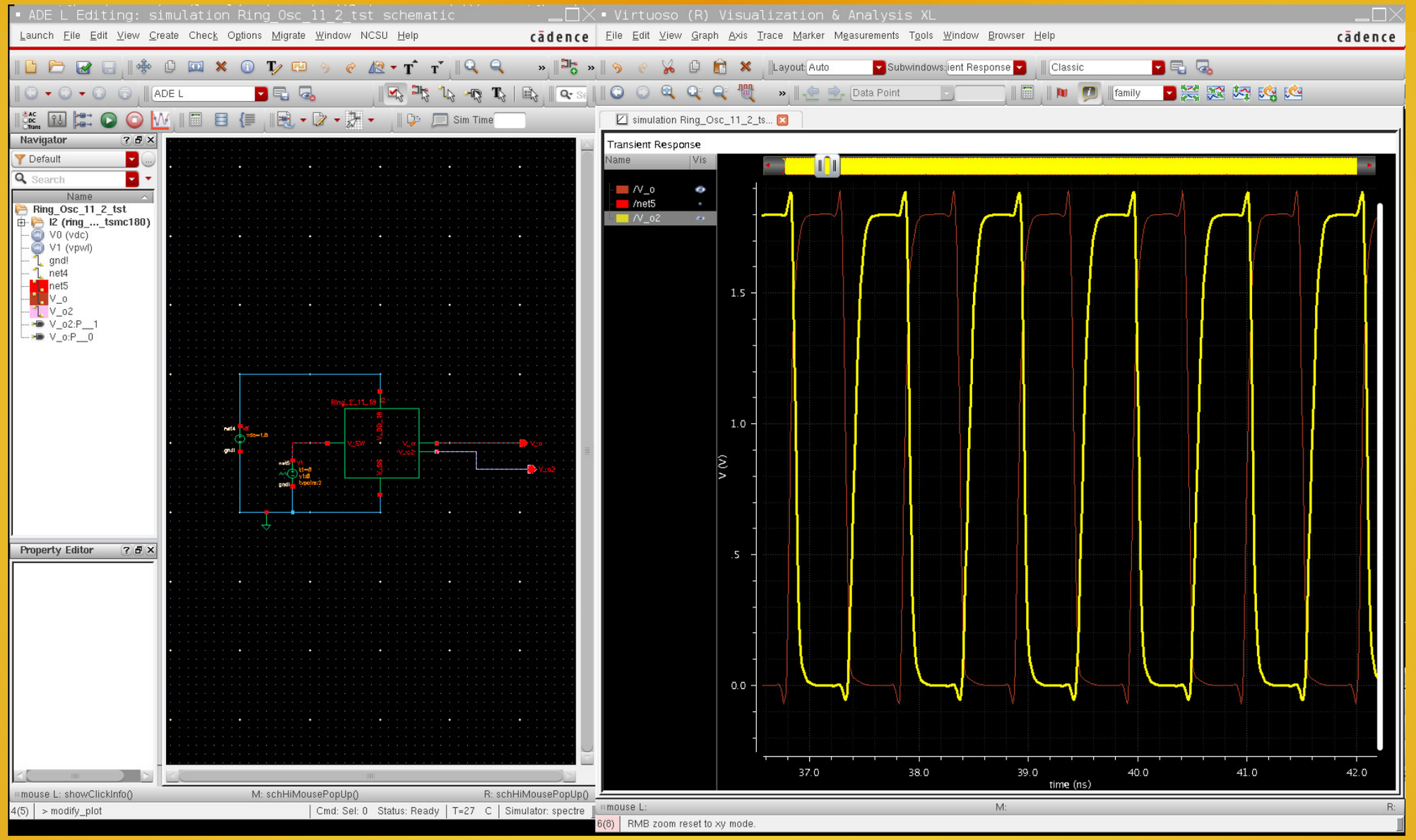




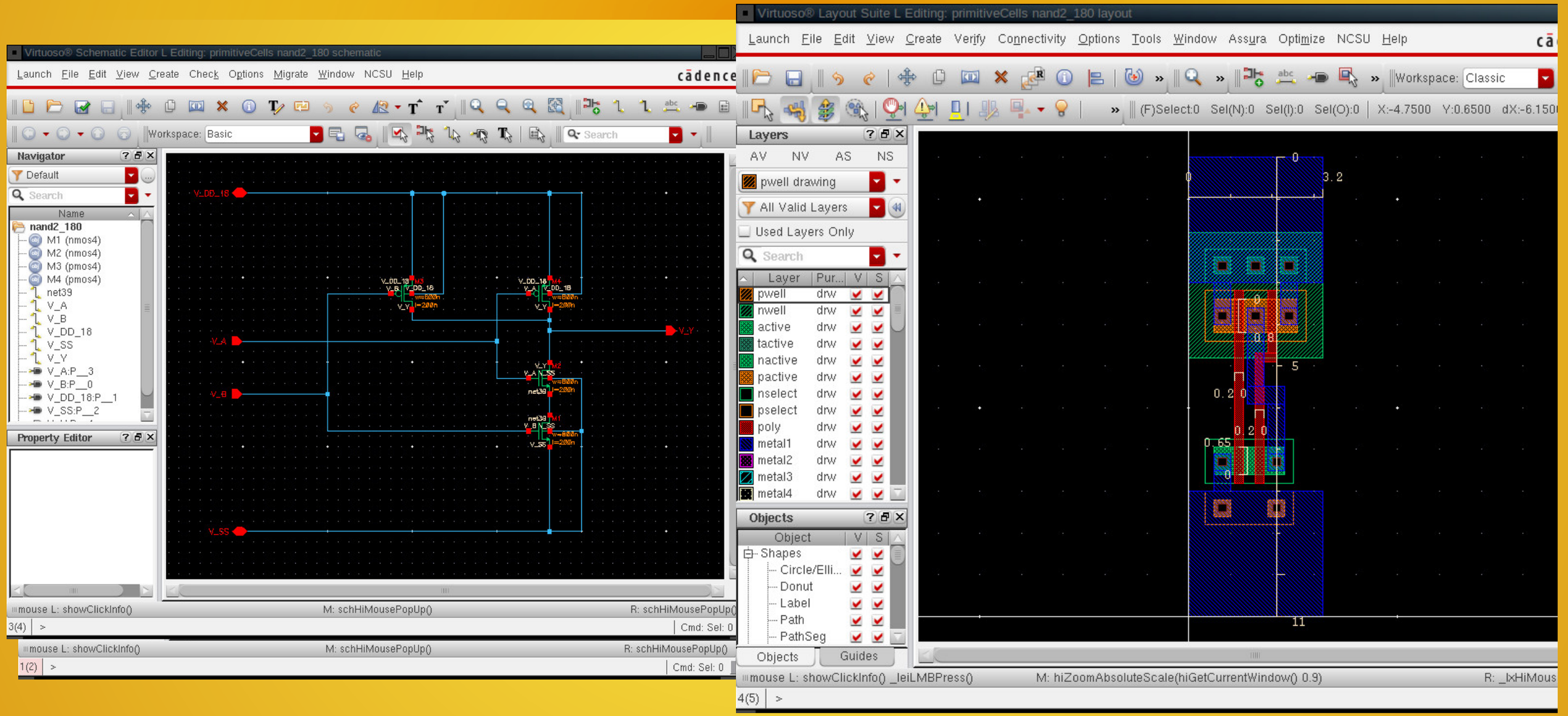
CMOS Inverter Transfer Characteristic Key: NO STANDBY POWER



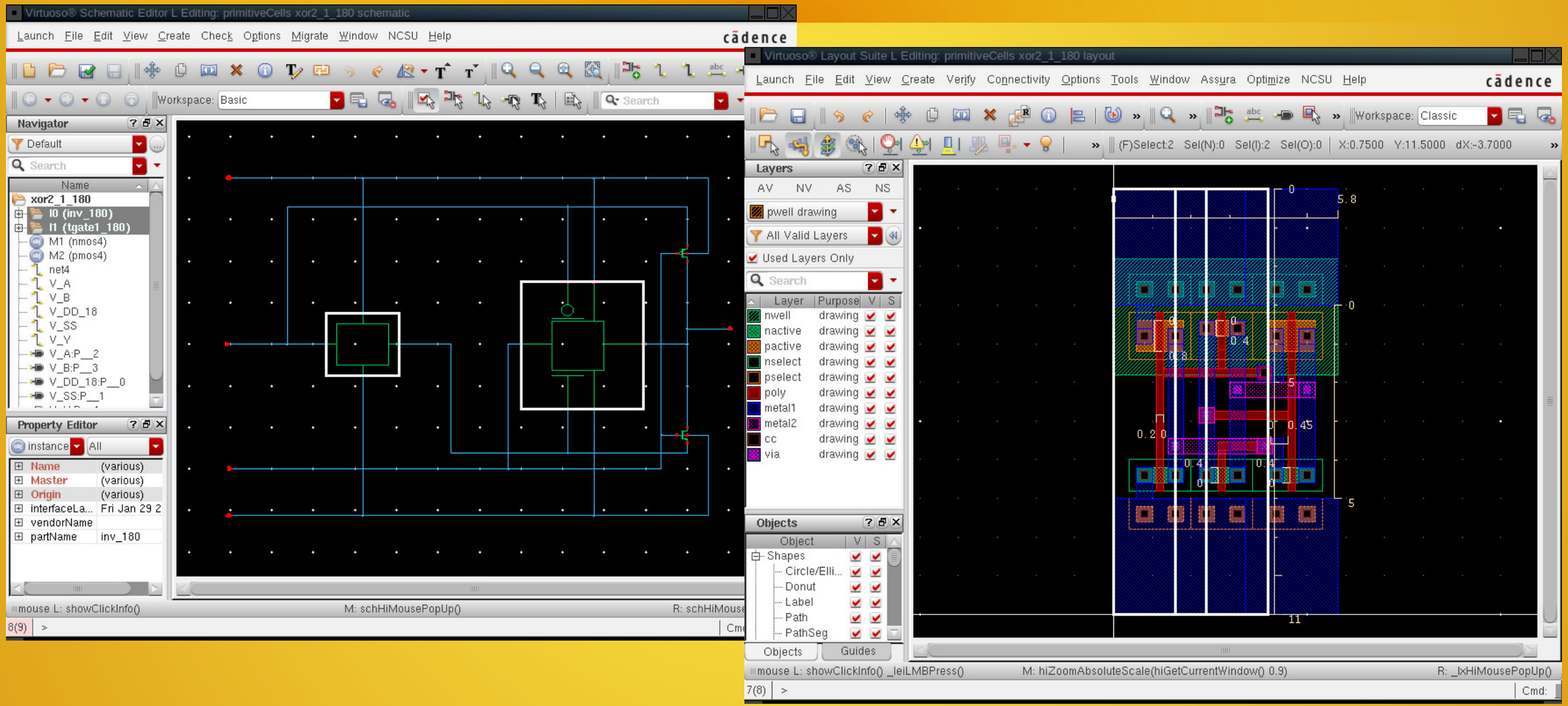
ADE Schematic Simulation



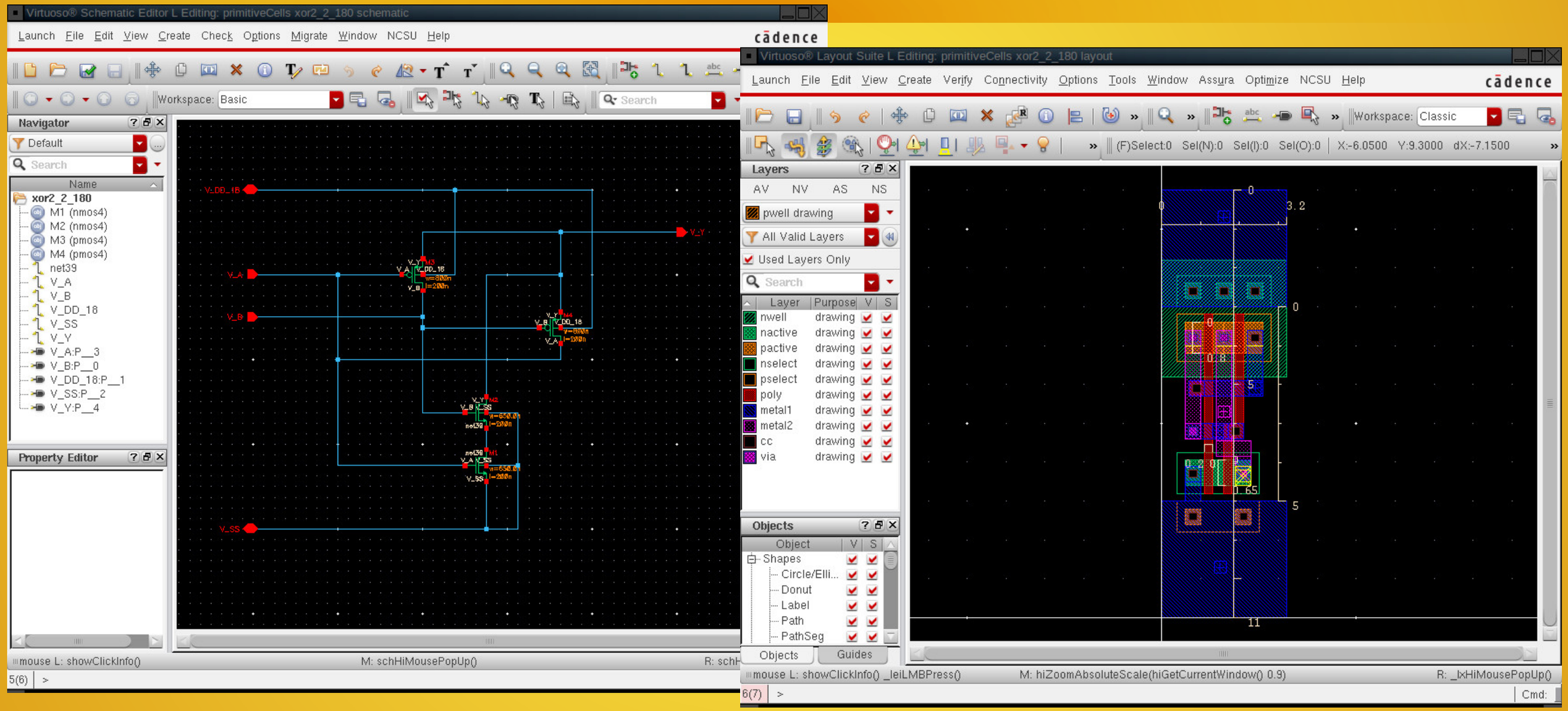
Virtuoso Schematic Editor & Layout Editor Example: Nand2 180nm



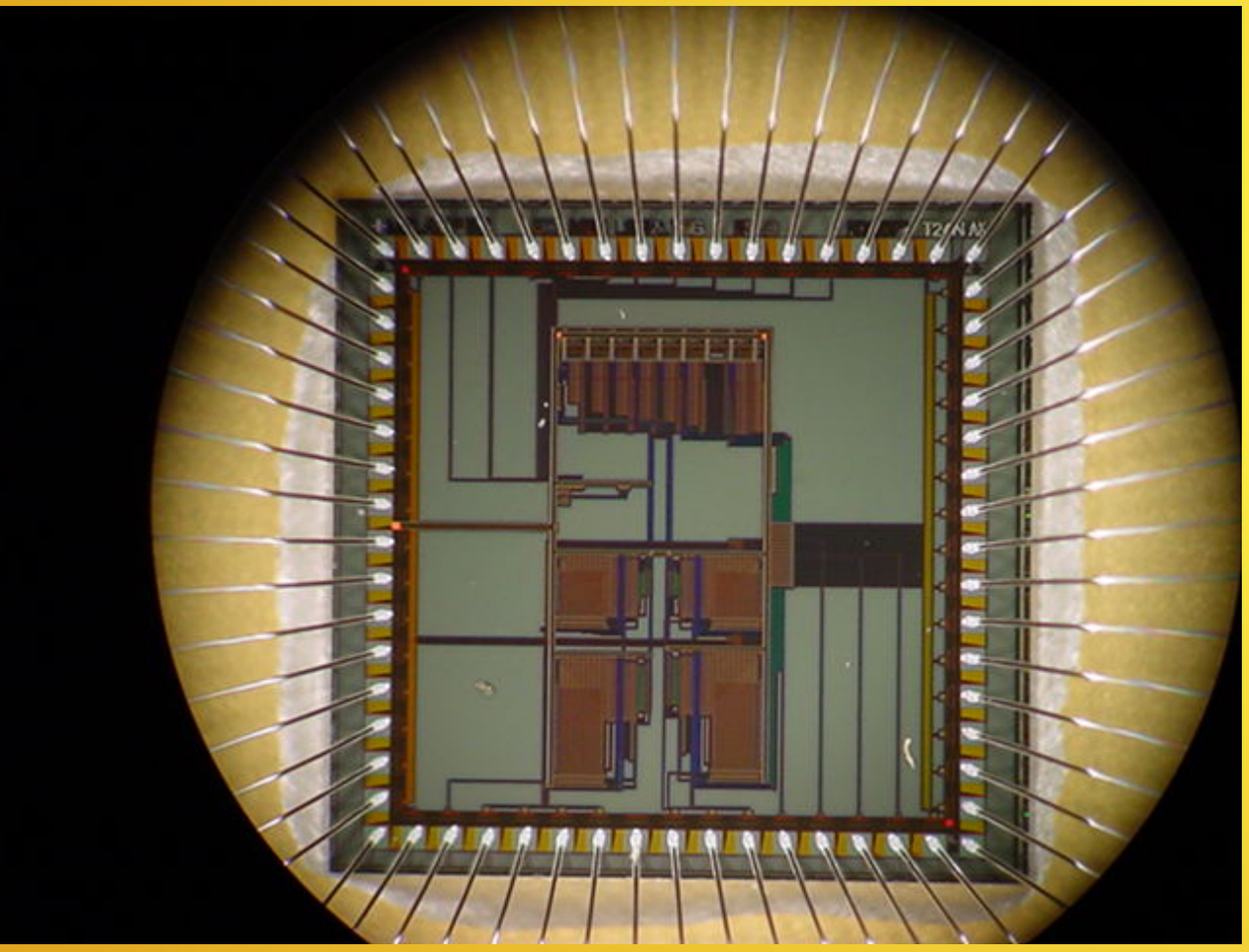
Virtuoso Schematic Editor & Layout Editor Example: xor2 6T 180nm

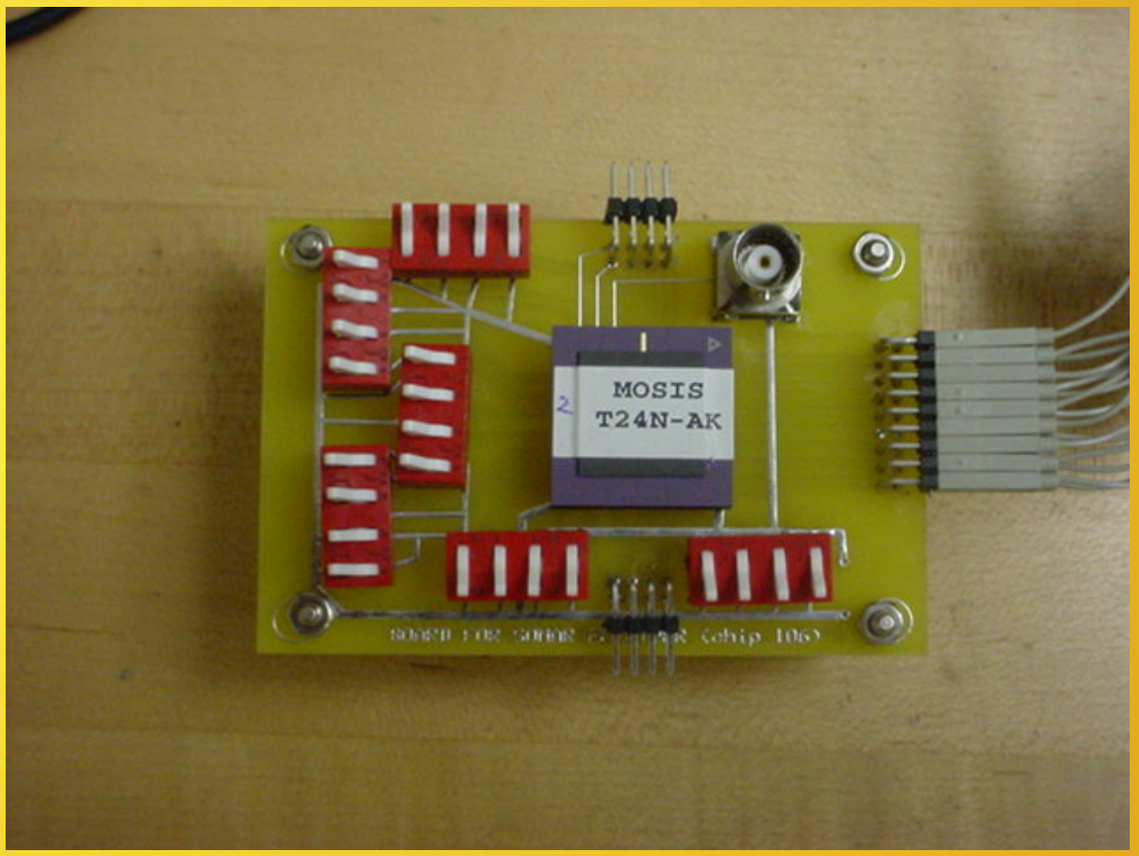


Virtuoso Schematic Editor & Layout Editor Example: xor2 4T 180nm



ICs Testing





Use Pseudo nMOS & CMOS Inverters to Introduce Static Logic Families

Electronics I (Linear Circuits, Current Source Models & Resistors)
Digital Integrated Circuit Design (Switch Models & Capacitive Loads)

- M2 is a Resistor or Current Source (Active)
- M1 is a Switch (Predominant Model)

- The Switch Output Can: Pull Up or Pull Down to either supply rail (or close to it)

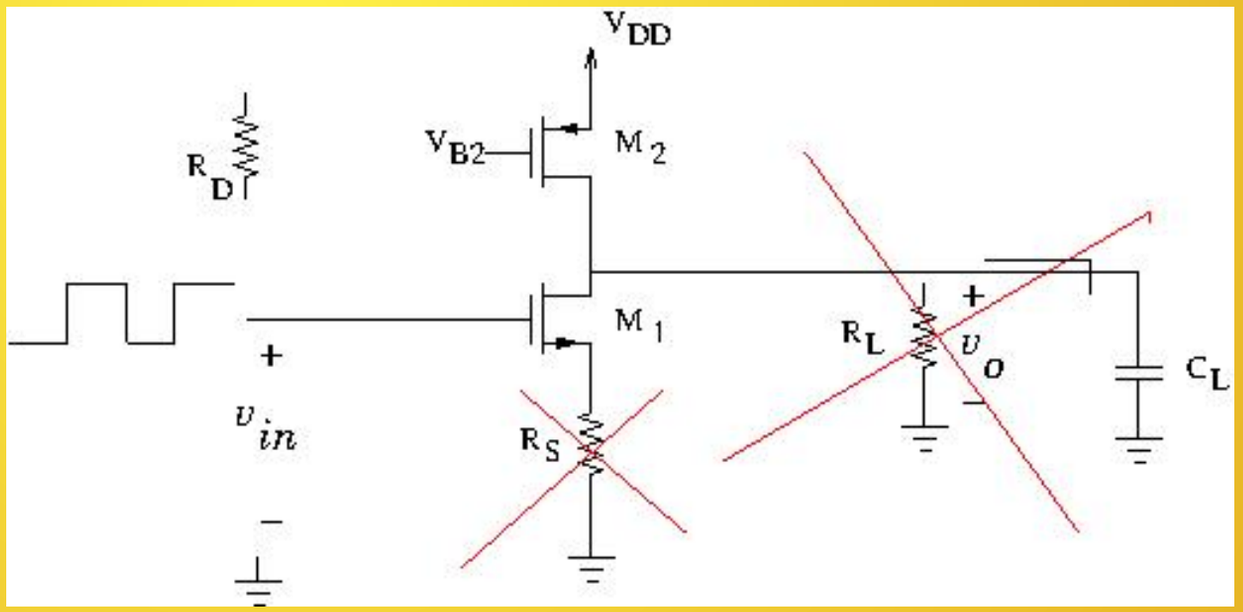
- Binary Switch States: ON/OFF

- Standard Analysis: RC Transient

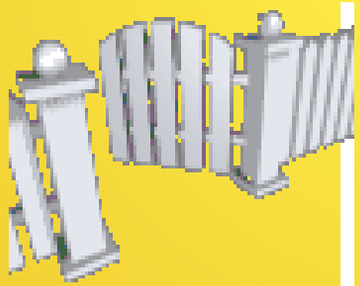
- Transistor → Resistor + Switch

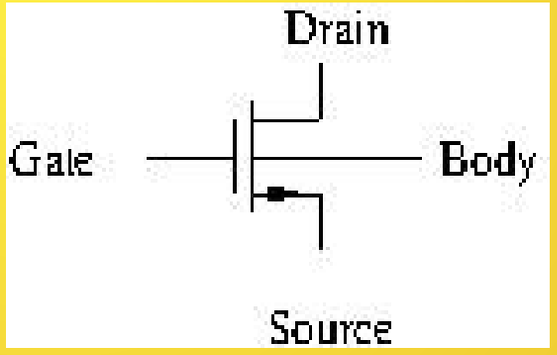
- Inputs/Outputs are Pulses, Not Sine Waves

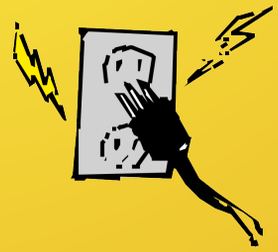
- 'Stability & Linearity' are traded for fast state changes (V_{DD}2Gnd; Gnd2V_{DD})



We Will Need to Think More About Device Physics/Models (vs Electronics)







URI Cad Tool Environment

Supporting IC Design Courses & Research

We will Need to Effectively use IC Design Tools

- Cadence
  - Virtuoso Schematic & Symbol Editor
  - Virtuoso Layout Editor
  - Analog Design Environment (ADE)
  - Spectre
  - Dracula, Assura & PVS: Design Rule Check (DRC) & Layout Vs. Schematic (LVS)
- Mentor Graphics
  - Calibre (DRC & LVS)
- Synopsys
  - Hspice
  - Cscope
  - TCAD Sentarus

Topics

- Switch Models for MOS Transistor Analysis/Synthesis
- RC Models/Transient Response for Timing Analysis
- Understanding Device Physics → Designer's Point of View
- Device Technology Scaling and its Implications on a Designer
- Synthesis of Basic Gates to Building Blocks (e.g. Adders, Mux's, etc.) to Systems To an Entire IC
- Detailed Study/Analysis of High-Speed Cells (usually one type/family)
- Overview of Highlighted System/Project
- Logic Families: Static CMOS, Pseudo nMOS, Dynamic Logic
- Circuit Simulation Tools → HSPICE and Spectre
- Design Flow → Cadence/Mentor Graphics
- Layout
- Verification
- Manufacturability, Reliability, Yield

Summary

- Our *Space* is Delivering a Layout with working circuitry → layout → reticle mask

- The *objective* is to understand the custom IC design process using automated CAD tools

- The Project Based Course: Grading will be based on: Labs, Hwk, Assignments and a Final Design Project

- Students will learn about the influence of device Physics on MOS transistors realized with smaller geometries (including non-ideal effects) from a *designer's point of view*

- Students are expected to understand basic circuit analysis, Emag(PH204) and Electronics I (ELE212/215; ELE 338/339)

- A basic understanding of digital logic, e.g. gates, latches, flip-flops, counters, adders, etc. is also required (ELE 201/202)