

Overview of Digital Integrated Circuit Design I



Course Objectives

- *Fabless* Digital IC Design
- **Design/Layout/Verification** of Hand-Crafted Transistors (e.g. **Primitive Cell Library**)
- Design/Layout/Verification of Functional Circuits Realized with Primitive Cells
- Synthesis of Complex Digital Systems Based on this Hierarchy
- Efficient use of CAD Tools Hosted in Linux
- End Product: *MPW Submission: GDS file(s)* → *Pure Play Foundry*
- Design/Project Based Course

- Course Sequence:
 - ELE 447/448 Digital IC Design I
 - ELE 537 Digital IC Design II (prereq: 447/448)
 - ELE 539 Analog IC Design (prereq: 447/448)

Semiconductor Foundries

- **Foundry Products: Processed Wafers !!! Reticle Masks are key to wafer processing (Foundry: Masks → Wafer Lots)**

- **Designer Produces a Layout (Mask Geometries) for die; Mask Shop Stitches die Layouts → Reticle Mask**

- A 'chip' is usually a packaged die: 'Chip 2 Product': Wafers → die are cut from wafers → die are then packaged

- 2 Major Business Models: Integrated Device Manufacturer (IDM) & Pure Play

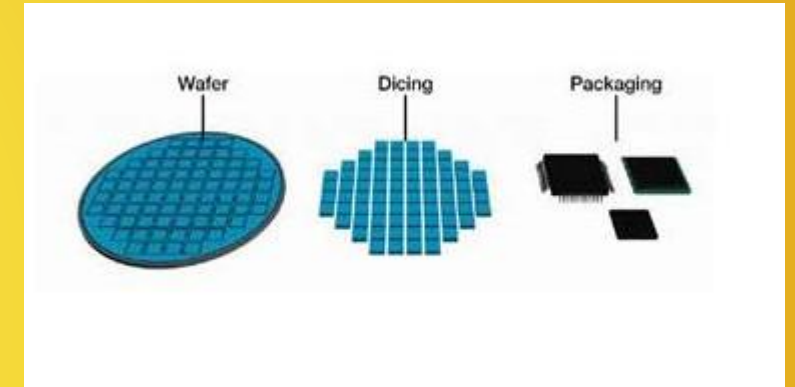
- Volume Business Regardless of the Business Model
- Economics drive the development & longevity
- Huge Capital Investments are Required: \$10 Billion or more, in some cases
- Global Business: Tools & Contracted Services

- IDM: A foundry that fabricates internally developed designs

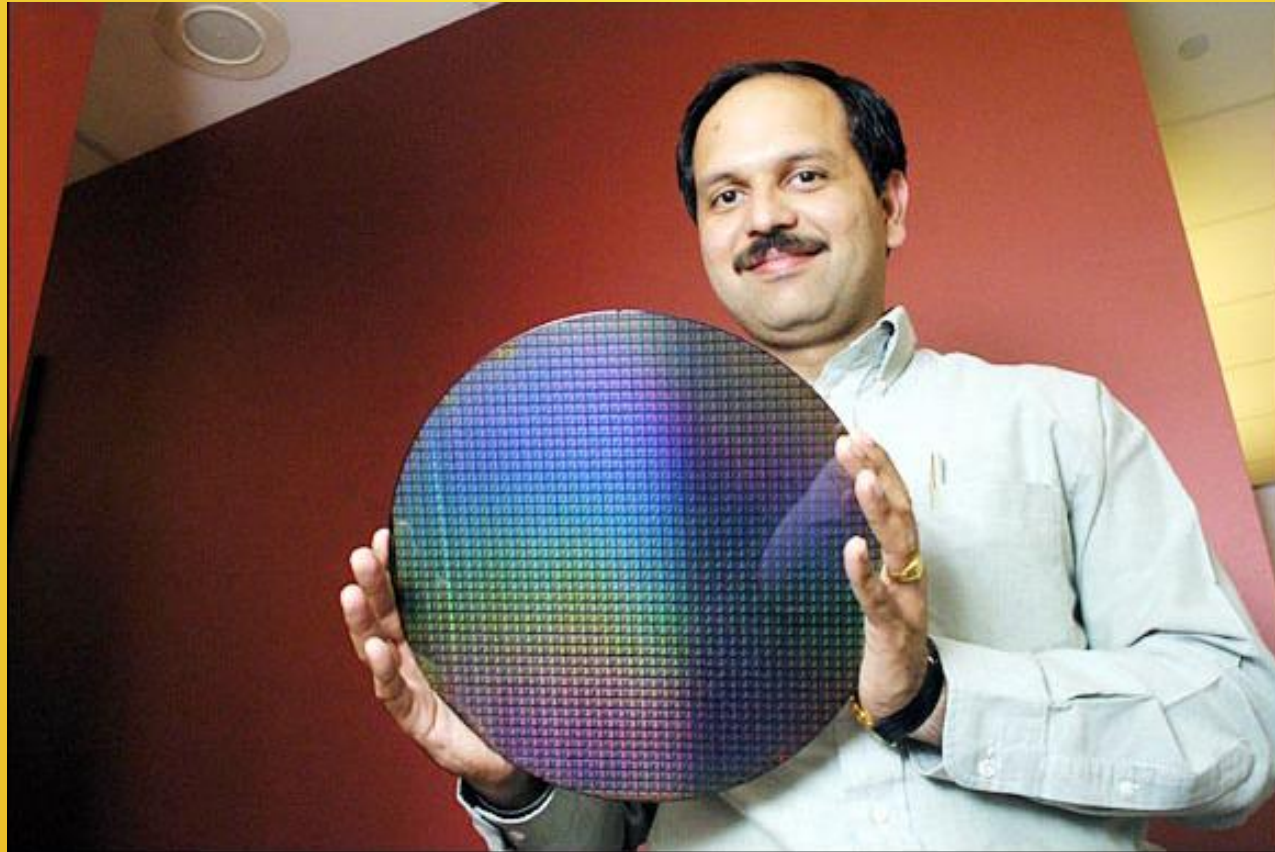
- Vertically Integrated from Designers to the Fabrication Lines; Designs are controlled by Foundry Employees ONLY
- Internally Developed CAD Tools(at least some); Customization & Foundry Integration are 'tight'
- IDMs sell 'packaged chips'; IDM Customers Buy the 'chips' it manufactures
- IDM Examples: Intel Corp., Samsung, TI

- Pure Play (or Merchant) Foundry: A foundry that fabricates designs for others

- Products are the use of the fabrication process & knowledge of the best methods
- Pure Play Foundries Sell Wafers; Customers buy Wafers (containing the customer's designs)
- CAD design interface must be distributed to customers → Infrastructure Required to Distribute Foundry Access
- Customers dice wafers, then package & sell 'chips' manufactured by the Pure Play Foundry
- Earliest Formal Example of a Pure Play 'Ecosystem': The MOSIS Service (1980; DARPA)
- Pure Play Examples: Taiwan Semiconductor Corp (TSMC), Global Foundries (GF), Tower Semiconductor



Typical CMOS Foundry Wafers are 200mm & 300mm: IBM 300 mm Wafer

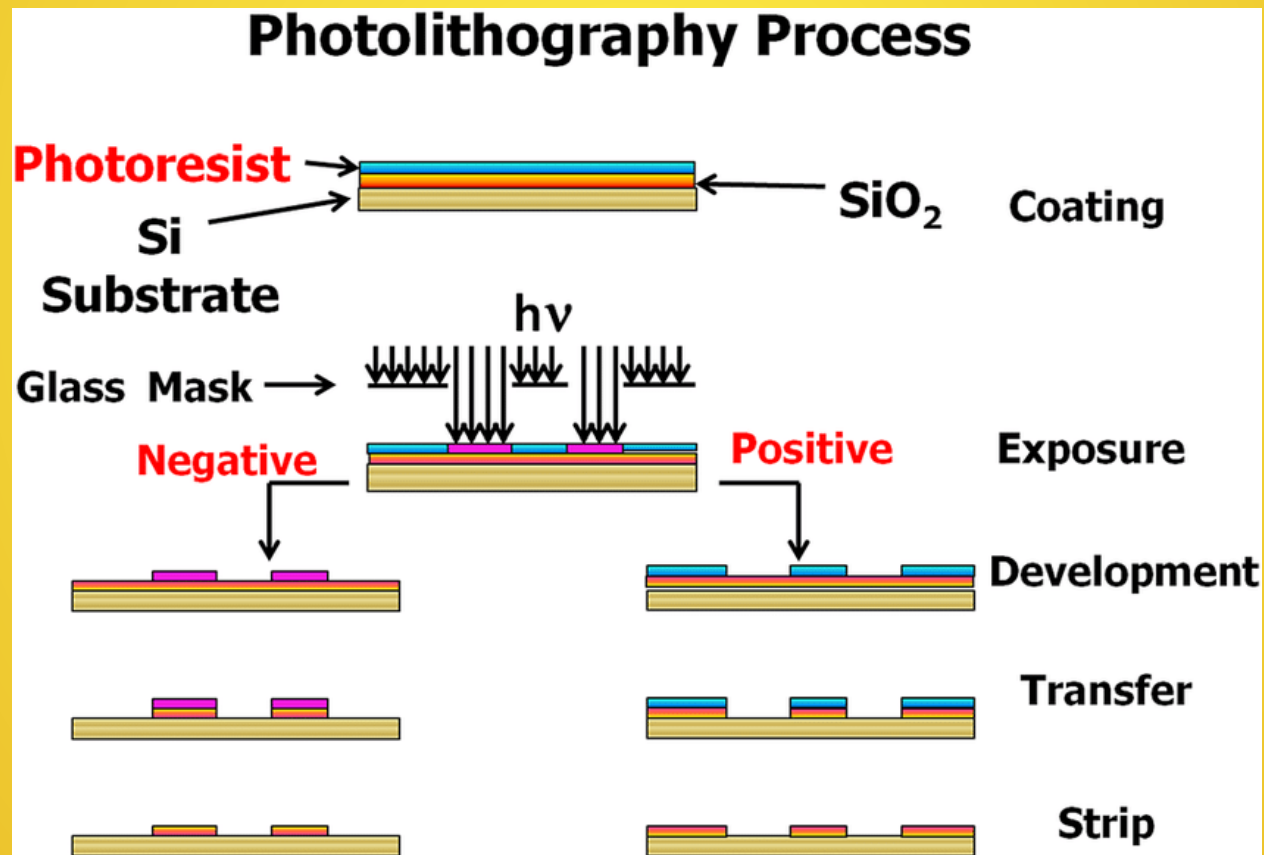


Pure Play Foundry Model

- Pure Play Customers: Fabless companies, device mfg's, Government labs, universities, even other foundries
 - Capital investments are minimized; so the customer can be a small business
 - The Customer must have knowledge about the Foundry Process Technology
 - The Customer is making a custom design
- Steps (Enablement: 1 &2):
 - 1- Non-disclosure agreement (NDA) signed by customer & foundry
 - 2- Foundry supplies process design kit (PDK) to customer; the PDK is usually DATA
 - 3- Customer uses PDK to generate a gds file containing layout(s)
 - 4- Foundry fabricates wafers from gds file supplied by customer(s)
 - 5- Wafers are delivered to the customer
 - 6- Wafers are tested and/or diced & tested on a board level
- Rules/Ethical/Legal Considerations
 - The NDA is a Legally Binding Document for both the Foundry & the Customer
 - The PDK is **Intellectual Property** owned by the Foundry & Is **Proprietary** (so, it cannot be 'shared' without the Permission of the Foundry; *even if the party sharing has an NDA !*)
 - The Customer agrees (*in the NDA*) to **Protect the PDK DATA & Documentation**
 - The Foundry agrees (*in the NDA*) to Protect the customer's **Design Submission DATA** (The Foundry goes to great lengths to prevent 'sharing' of customer data)
- Violations of the 'Rules' Can Result in:
 - Fines, Law Suits & other Civil Actions
 - Criminal Charges
 - Severe Damage to a Company's or Individual's Reputation
 - Loss of Customer Base (which the Foundry Needs to exist)

Photolithography → Selection Using Mask

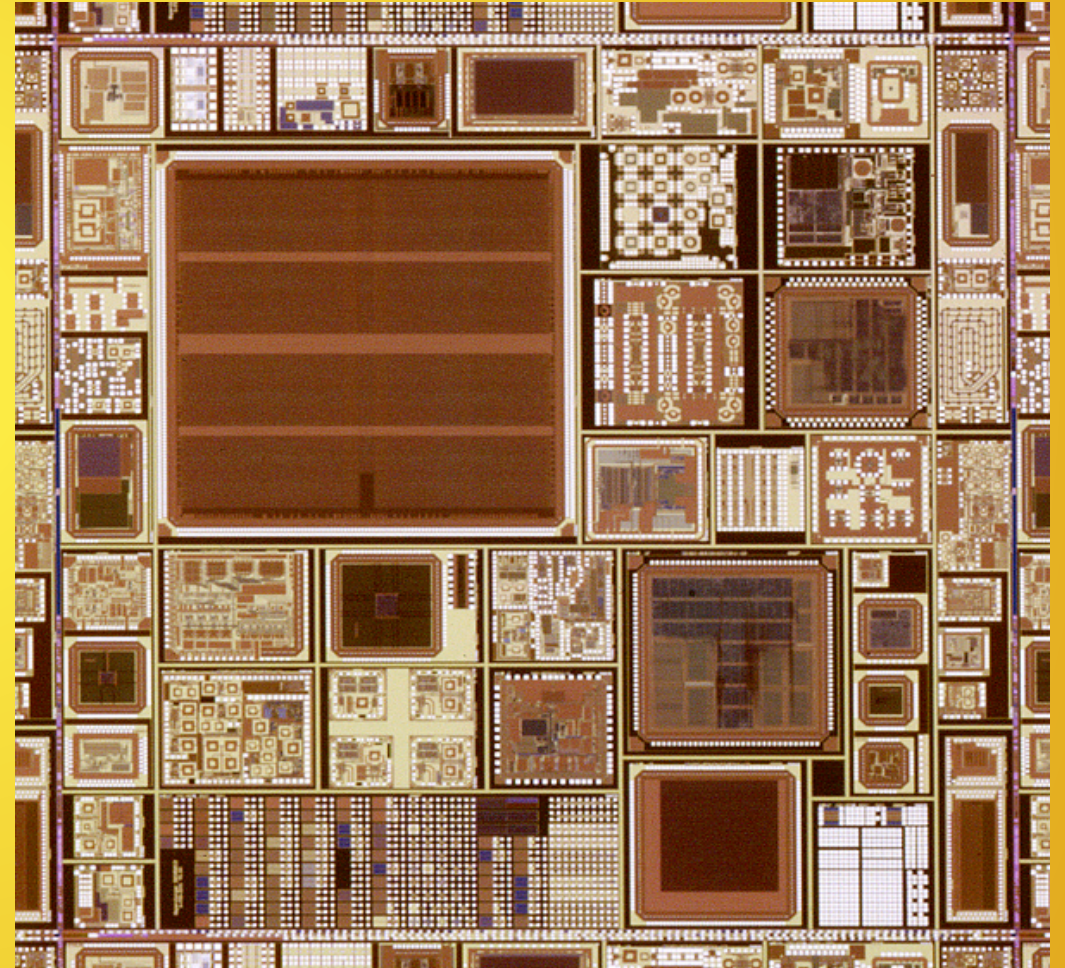
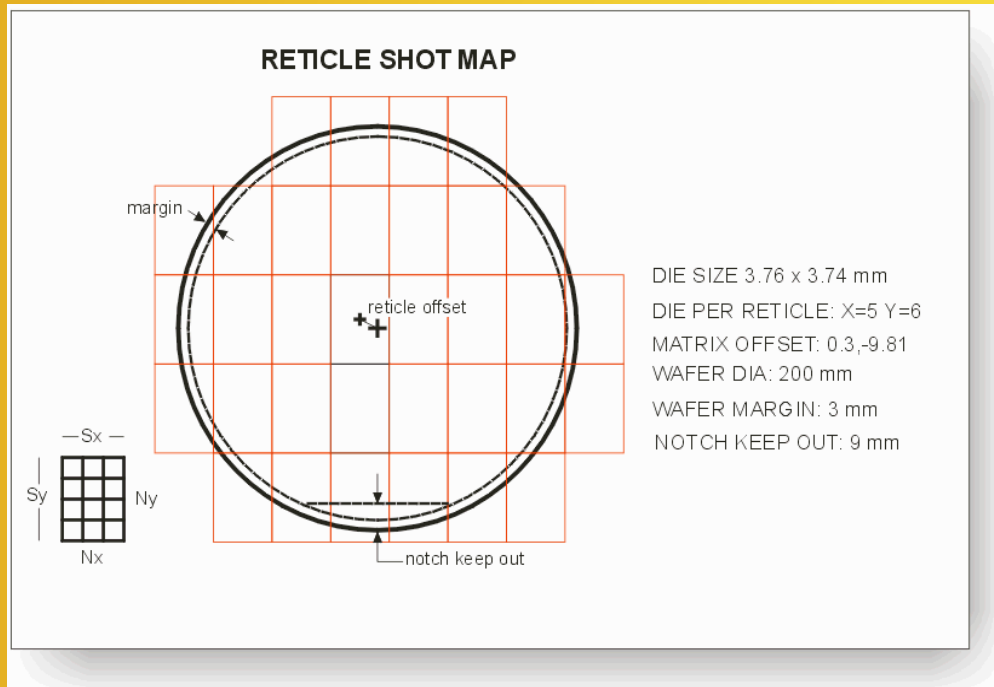
This is done at least 1x for each processing step (1 of 30-100 steps)
The Layout Contains a Complete Set of Masks for a Particular Design



What is in a PDK ?/How is it used ?

- Process Design Kit (PDK) Contents (**PROPRIETARY: Intellectual Property of the Foundry !!!**)
 - SPICE Circuit Models of key devices
 - Technology files
 - ALL Mask Layers (pseudo & real)
 - Design Rules for the Mask Layers
 - Rules for Layout vs. Schematic (LVS)
 - Design Manual & other documentation
 - ESD Guidance
 - Test results from wafers & devices
- PDK is integrated into the CAD Tool
 - PDK Data is integrated into the CAD Tool software (by the user)
 - CAD Tool environment will adapt & morph into the PDK's environment
 - ONLY CAD Tools supported by the foundry can use the PDK
- PDK functions
 - Simulation of Circuit Design
 - Layout Generation
 - Design Verification
 - Generation of GDS files for design submission

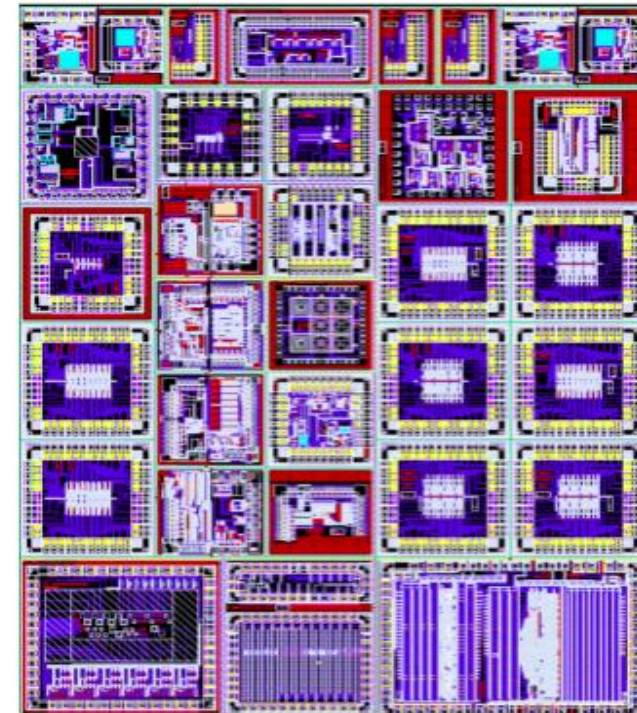
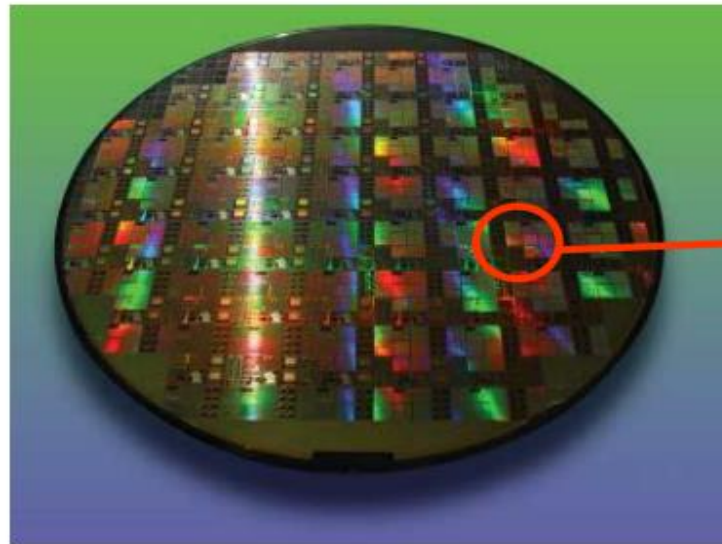
What is an MPW & Picture of MPW Reticle



- Pure Play (or Merchant) Foundry: Multi-Project Wafer (MPW)
- Pure Play Foundry Wafers can Contain a Single Dedicated Design or Multiple Customer Designs
- Multi-Project Wafers are a 2nd 'ary product: Shared cost for prototyping

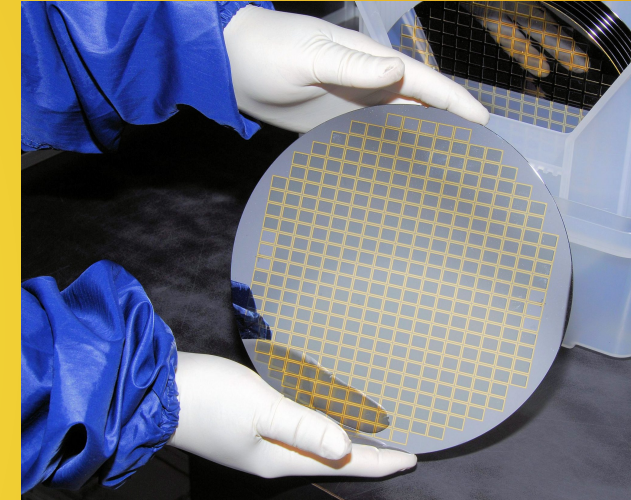
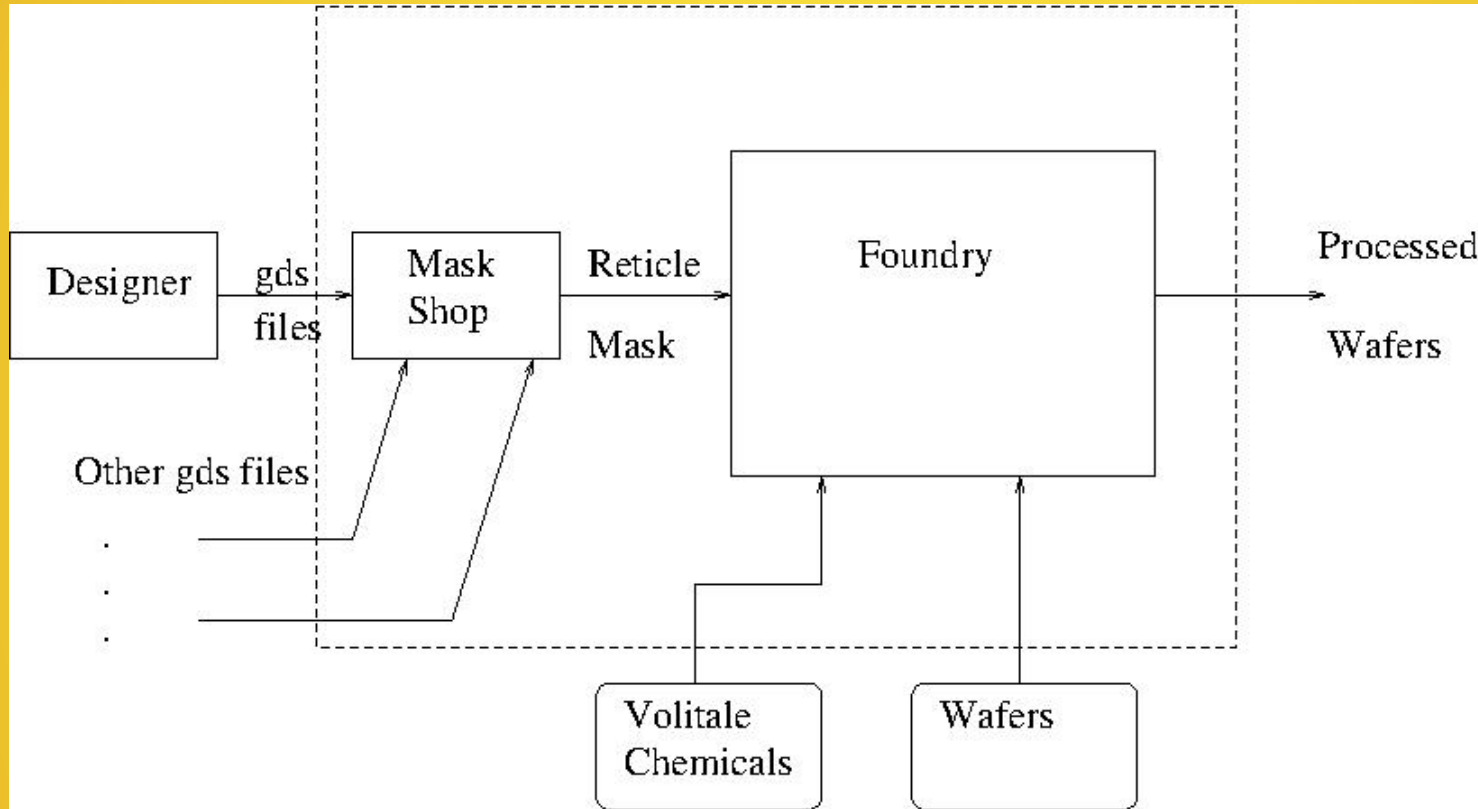
Multi-Project Wafers

- Mask set cost: >\$1M for 90 nm technology
- **Share cost of mask tooling between multiple designs!**
 - Prototyping
 - Low volume production



Summary of Wafer Fabrication Process

Dedicated Wafer run would repeat the same die layout from a single gds file; An MPW would integrate multiple die layouts contained in multiple gds files from different designers

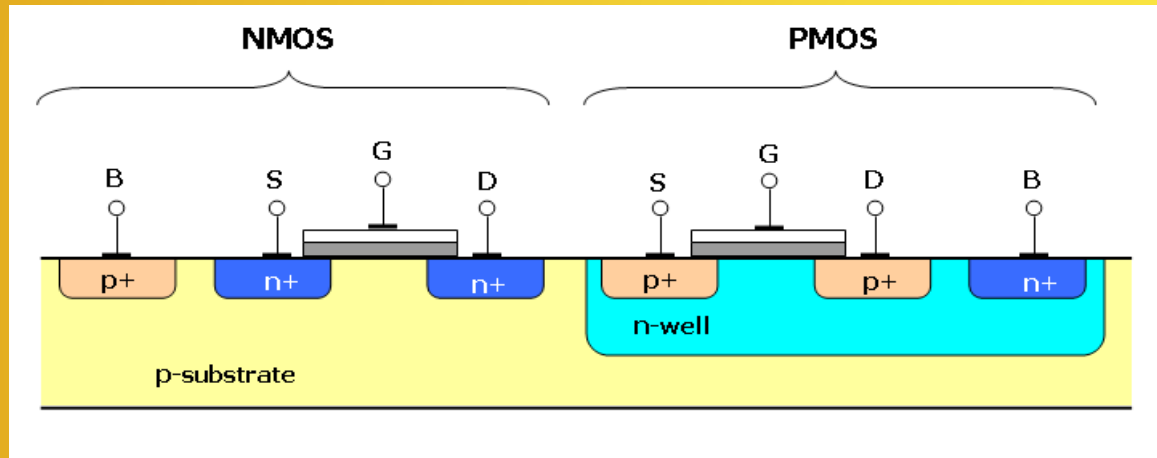


More volatile chemicals than used by both of these characters combined

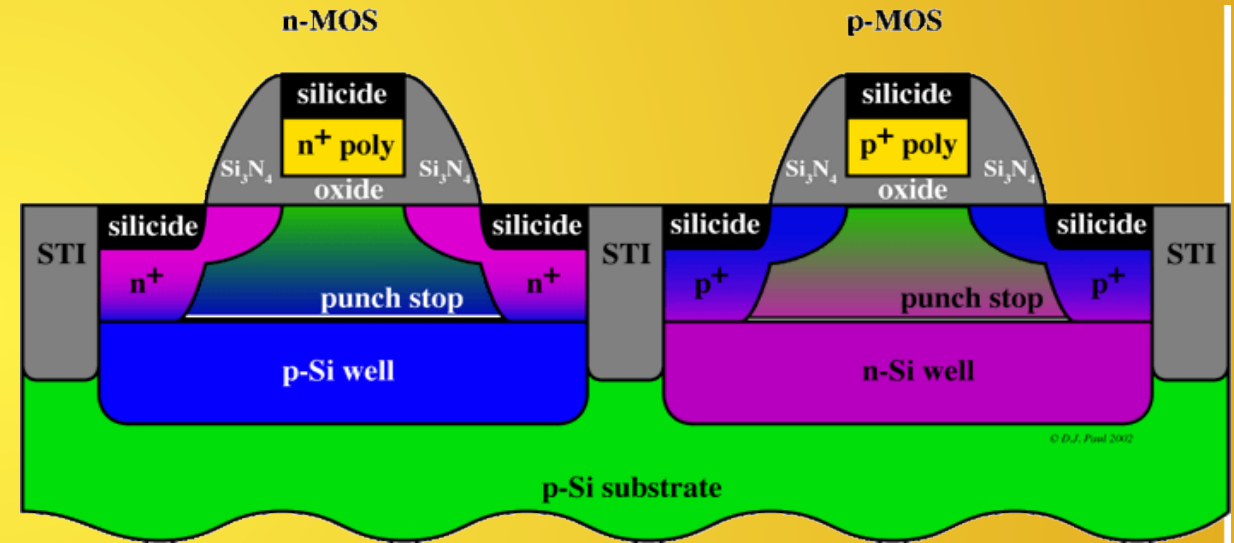


Blank/pre-doped wafers are supplied by vendor(s)

Bulk CMOS Cross Sections



Simple



Detailed (no Body Contact Shown)

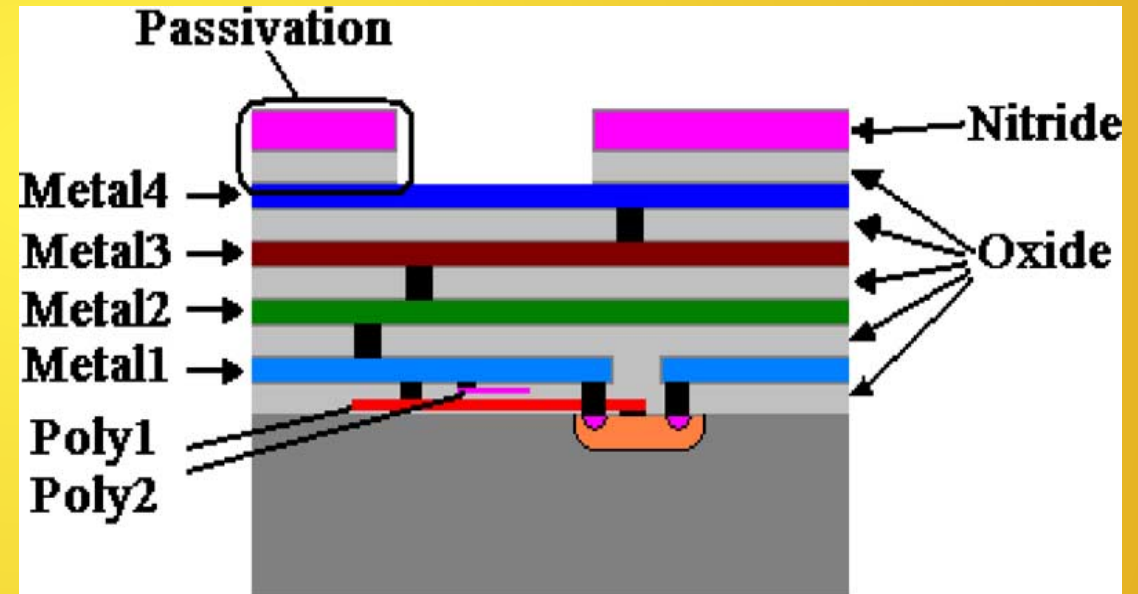
Metal Stacks

(Processes Often Provide Several Metal Stack Options)



Metal Stacks for 130nm thru 32 nm

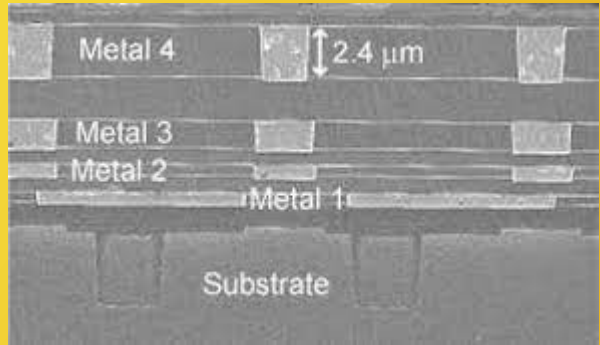
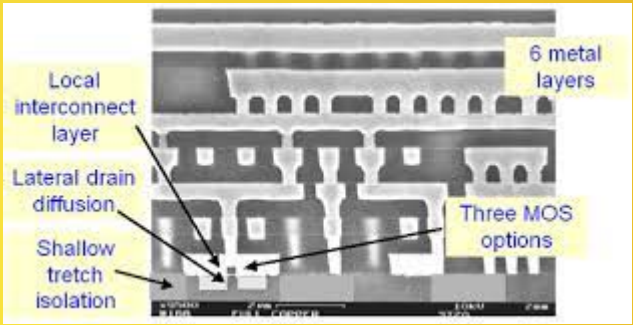
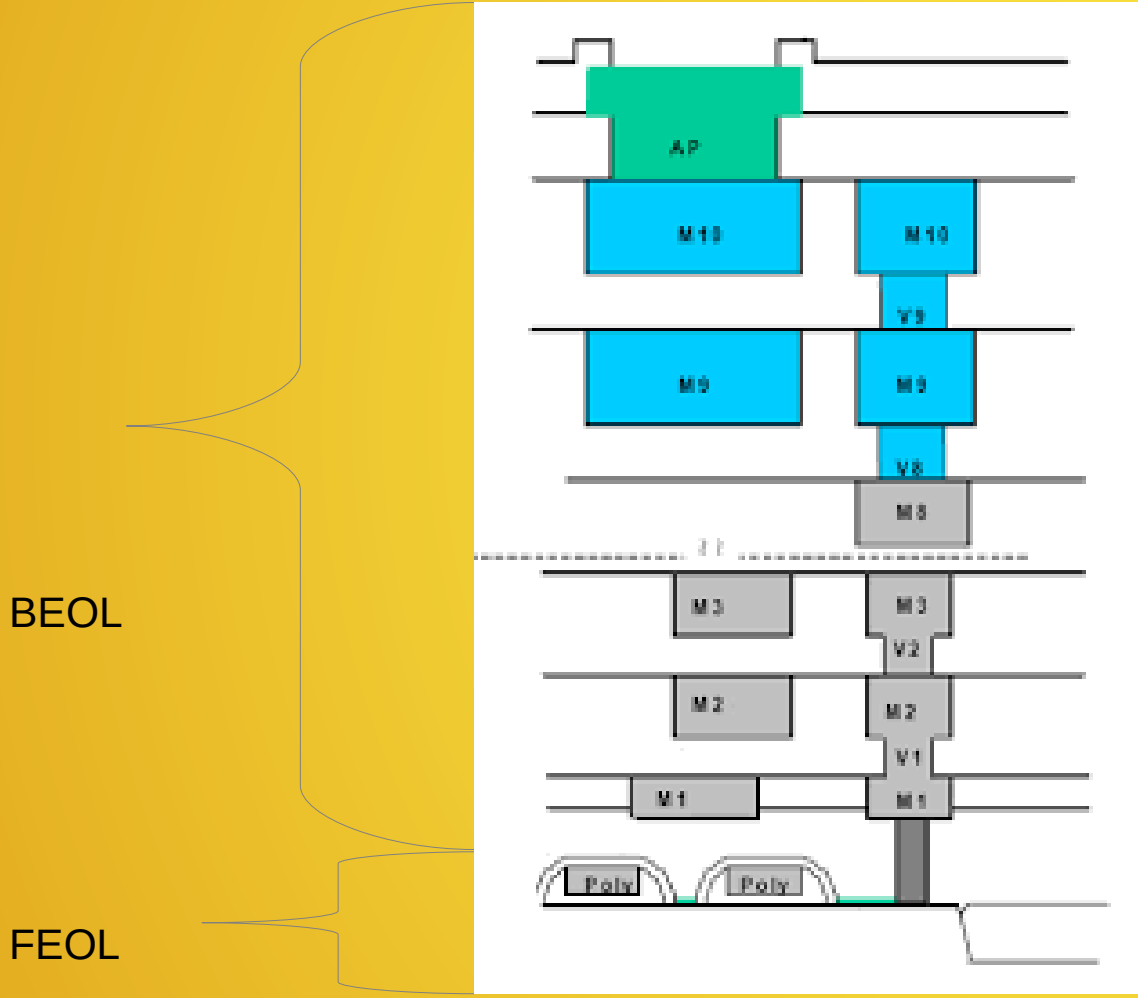
(caps, resistors & inductors can be implemented)



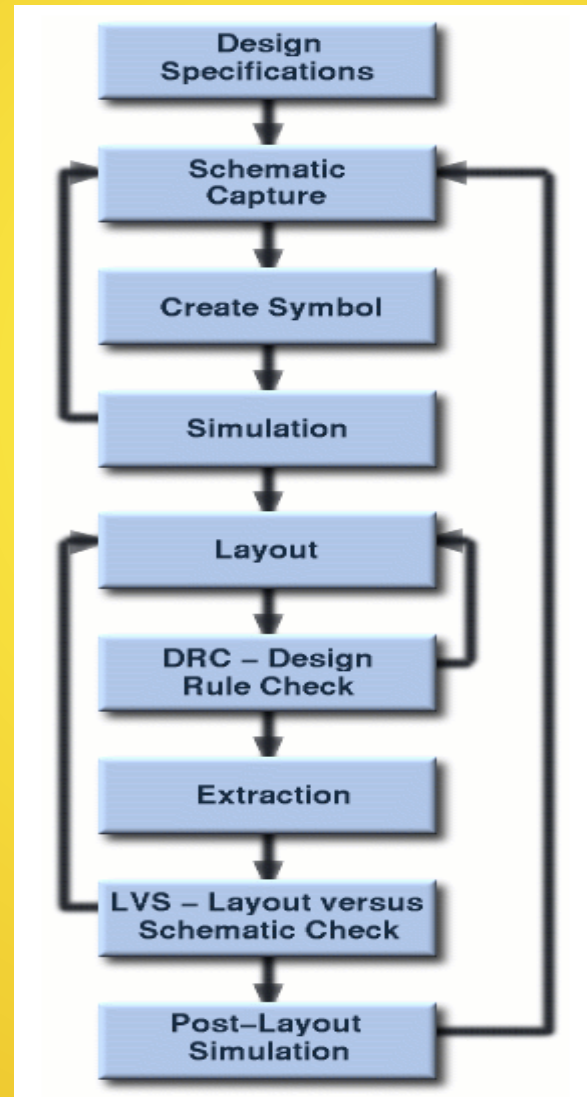
Example of Metal Stack with 2 Poly Layers

Caps can be realized with 2 poly layers

180nm SiGe BiCMOS with FEOL & BEOL



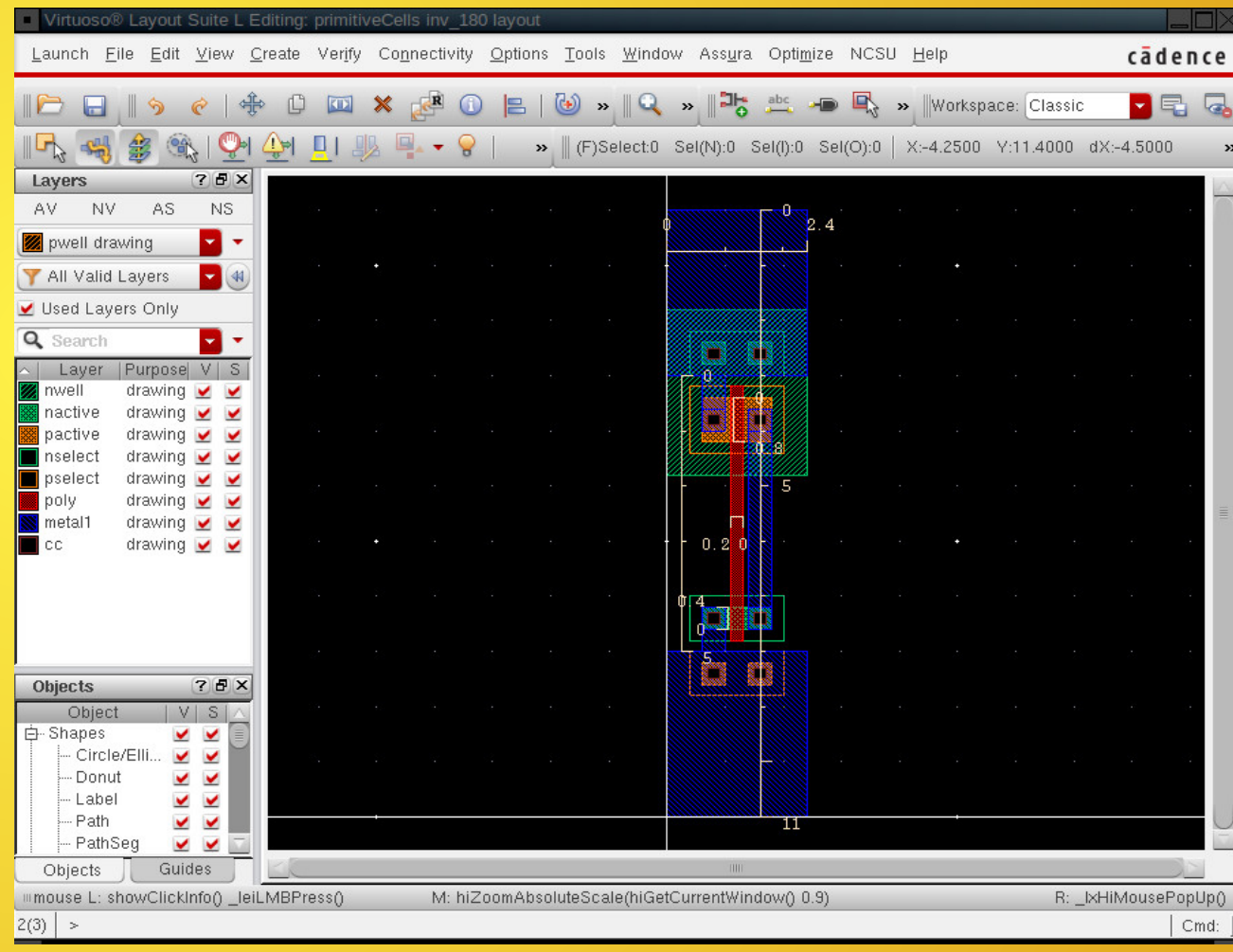
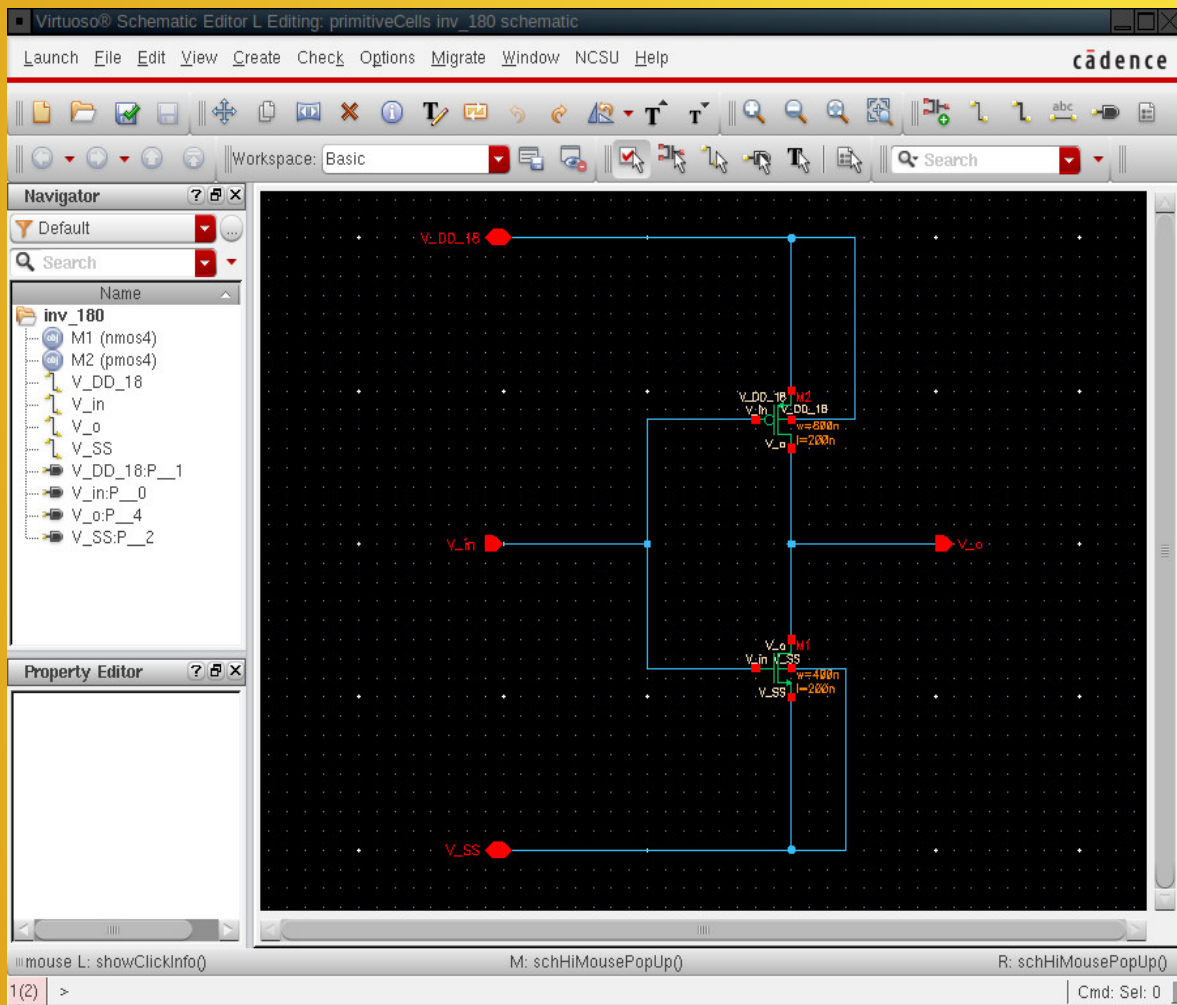
Design Flow



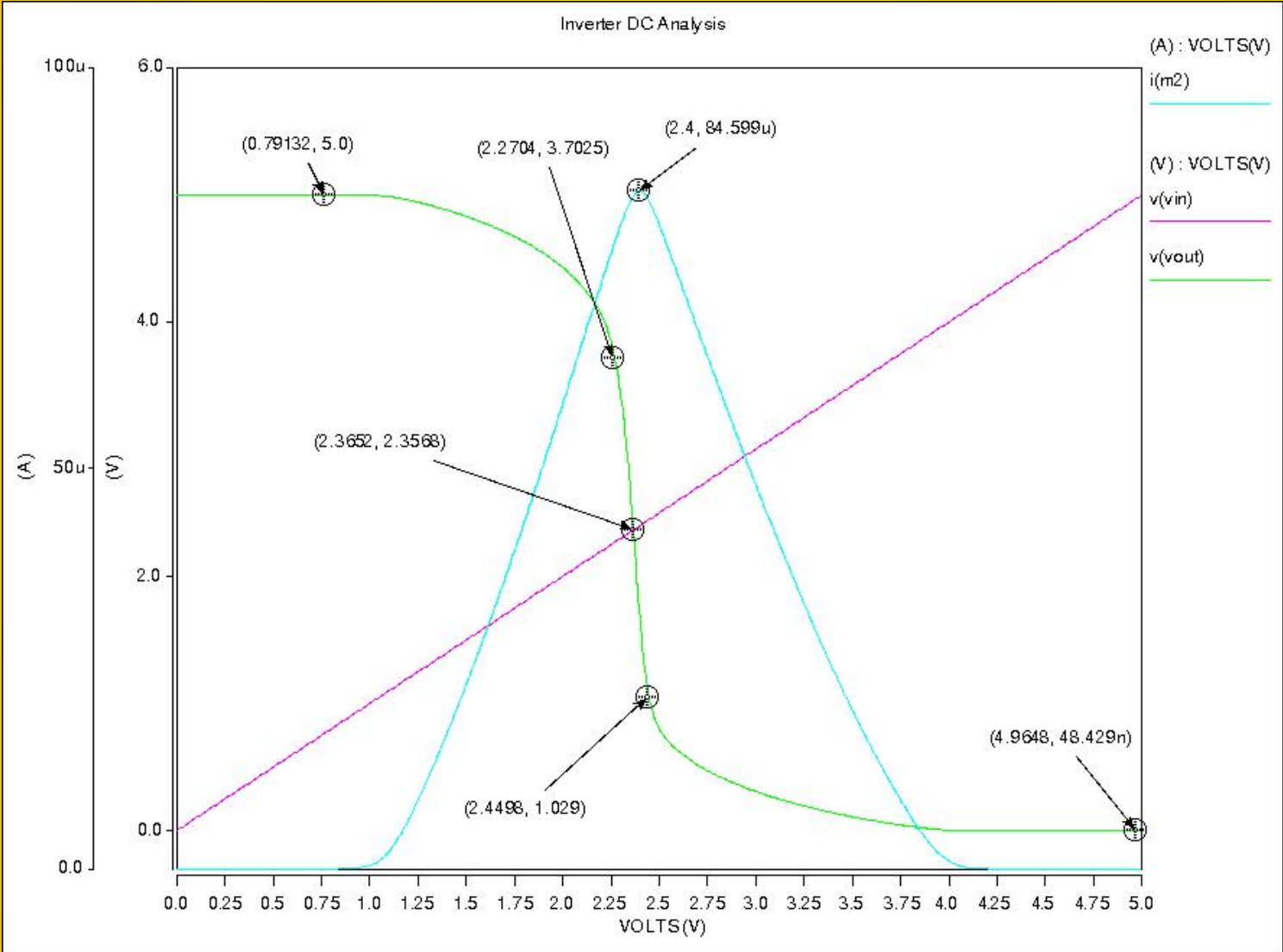
Hierarchy & Reuse

| | |
|------------------------|--|
| Level N | <hr/> Top Level System <hr/> Cells are Used & Reused whenever possible <ul style="list-style-type: none">••• <hr/> |
| Level 1 | <hr/> Counters, registers, adders, ..., all realized from Primitive Cells <hr/> |
| Primitive Cells | Primitive Cells Are Used & Reused basic logic, 1-bit dff's, 1-bit latches, 1-bit adders, etc. |

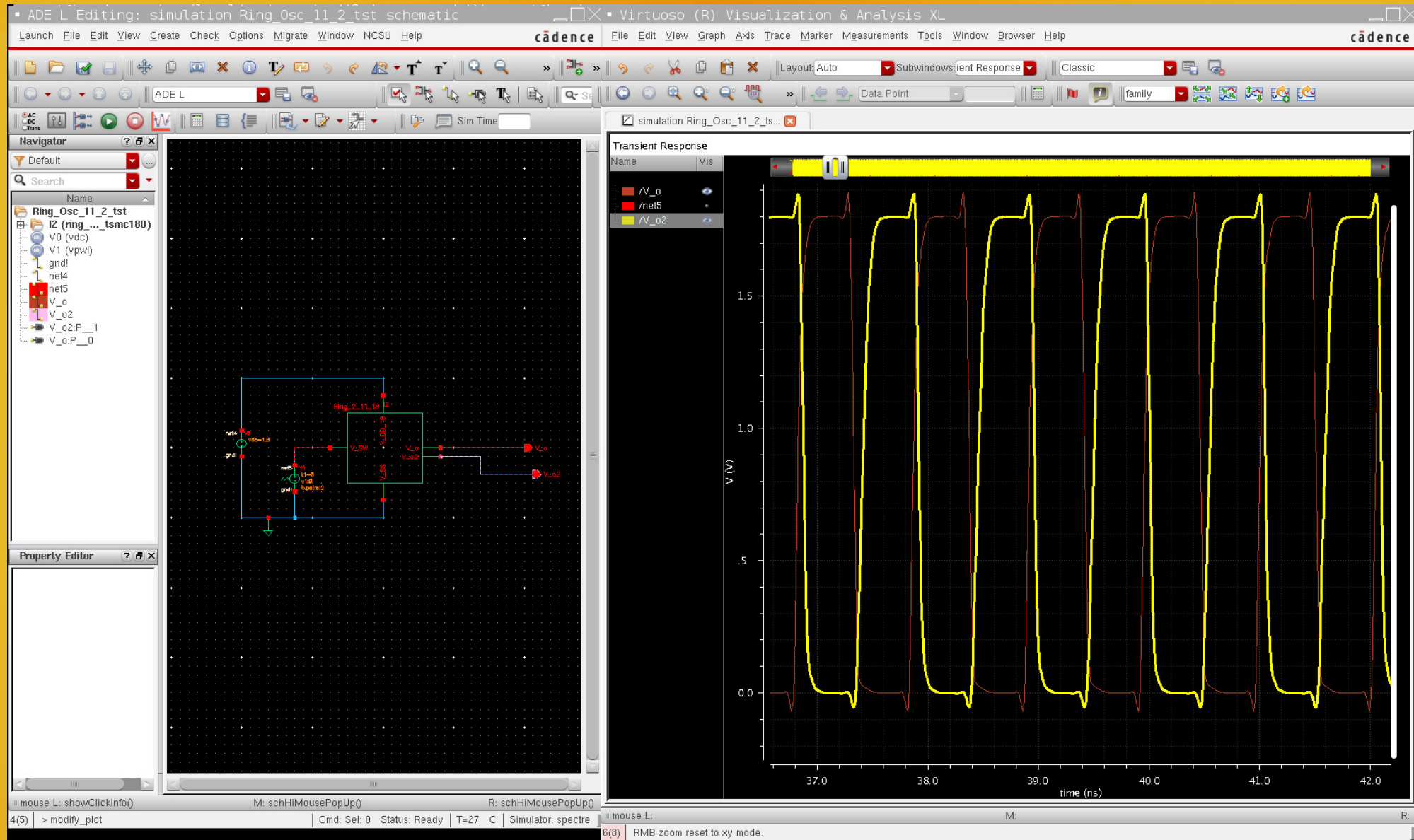
Virtuoso Schematic Editor & Layout Editor Example: Inverter 180nm



CMOS Inverter Transfer Characteristic Key: NO STANDBY POWER



ADE Schematic Simulation



Virtuoso Schematic Editor & Layout Editor Example: Nand2 180nm

The image displays two windows from the Cadence Virtuoso Layout Suite, illustrating the design of a Nand2 cell at 180nm technology.

Left Window: Schematic Editor
Title: Virtuoso® Schematic Editor L Editing: primitiveCells nand2_180 schematic
The schematic shows a NAND2 gate implementation. It features two input nodes, V_A and V_B, and one output node, V_Y. The circuit includes four NMOS transistors (M1, M2, M3, M4) and four PMOS transistors (M1, M2, M3, M4). The PMOS transistors are connected in series between V_DD_18 and V_SS. The NMOS transistors are connected in parallel between V_Y and V_SS. The schematic is annotated with various parameters such as W=800n, L=200n, and W=800n, L=200n.

Right Window: Layout Editor
Title: Virtuoso® Layout Suite L Editing: primitiveCells nand2_180 layout
The layout editor shows the physical implementation of the NAND2 gate. The layout is composed of various layers, including pwell, nwell, active, tactive, nactive, pactive, nselect, pselect, poly, metal1, metal2, metal3, and metal4. The layout is annotated with various parameters such as 0.2, 0.8, 0.65, 0, 11, and 3.2. The layout is shown in a top-down view, with the input and output pads clearly visible.

Layers Panel:

| Layer | Pur... | V | S |
|---------|--------|---|---|
| pwell | drw | ✓ | ✓ |
| nwell | drw | ✓ | ✓ |
| active | drw | ✓ | ✓ |
| tactive | drw | ✓ | ✓ |
| nactive | drw | ✓ | ✓ |
| pactive | drw | ✓ | ✓ |
| nselect | drw | ✓ | ✓ |
| pselect | drw | ✓ | ✓ |
| poly | drw | ✓ | ✓ |
| metal1 | drw | ✓ | ✓ |
| metal2 | drw | ✓ | ✓ |
| metal3 | drw | ✓ | ✓ |
| metal4 | drw | ✓ | ✓ |

Objects Panel:

| Object | V | S |
|-----------------|---|---|
| Shapes | ✓ | ✓ |
| Circle/Ellip... | ✓ | ✓ |
| Donut | ✓ | ✓ |
| Label | ✓ | ✓ |
| Path | ✓ | ✓ |
| PathSeg | ✓ | ✓ |

Virtuoso Schematic Editor & Layout Editor Example: xor2 6T 180nm

The image displays two windows from the Cadence Virtuoso suite, illustrating the design of an XOR gate (xor2) in a 6T180nm technology.

Left Window: Virtuoso® Schematic Editor L Editing: primitiveCells xor2_1_180 schematic

This window shows the schematic editor interface. The main workspace displays a circuit diagram of an XOR gate. The circuit consists of two NMOS transistors (M1 and M2) and two PMOS transistors (M3 and M4) connected in a 6T1 configuration. The schematic is overlaid on a grid. The Navigator panel on the left shows the hierarchy of the circuit, including the input nodes (I0, I1), the transistors (M1, M2), and the various power and signal nets (V_A, V_B, V_DD_18, V_SS, V_Y, V_A_P_2, V_B_P_3, V_DD_18:P_0, V_SS:P_1). The Property Editor at the bottom left shows the properties of the selected instance, including its name, master, origin, and part name (inv_180).

Right Window: Virtuoso® Layout Suite L Editing: primitiveCells xor2_1_180 layout

This window shows the layout editor interface. The main workspace displays the physical layout of the XOR gate. The layout is overlaid on a grid and shows the physical placement of the transistors, interconnects, and other layout elements. The Layers panel on the left shows the list of layers used in the layout, including nwell, nactive, pactive, nselect, pselect, poly, metal1, metal2, cc, and via. The Objects panel at the bottom shows the list of objects used in the layout, including Shapes, Circle/Ellipse, Donut, Label, Path, and PathSeg. The status bar at the bottom right shows the coordinates of the selected object: X:0.7500 Y:11.5000 dX:-3.7000.

Virtuoso Schematic Editor & Layout Editor Example: xor2 4T 180nm

The image displays two windows from the Cadence Virtuoso suite, illustrating the design of a 4T 180nm XOR gate.

Left Window: Virtuoso® Schematic Editor L Editing: primitiveCells xor2_2_180 schematic

This window shows the schematic of the XOR gate. The circuit includes four transistors (M1, M2, M3, M4) and various power and signal nodes. The input nodes are V_A and V_B, and the output node is V_Y. The power supply nodes are V_DD_18 and V_SS. The schematic is connected to a grid with dimensions of 650.0 and 200.0.

Right Window: Virtuoso® Layout Suite L Editing: primitiveCells xor2_2_180 layout

This window shows the physical layout of the XOR gate. The layout is composed of various layers, including nwell, nactive, pactive, nselect, pselect, poly, metal1, metal2, cc, and via. The layout is shown on a grid with dimensions of 650.0 and 200.0. The layout is color-coded to show different layers and their purposes.

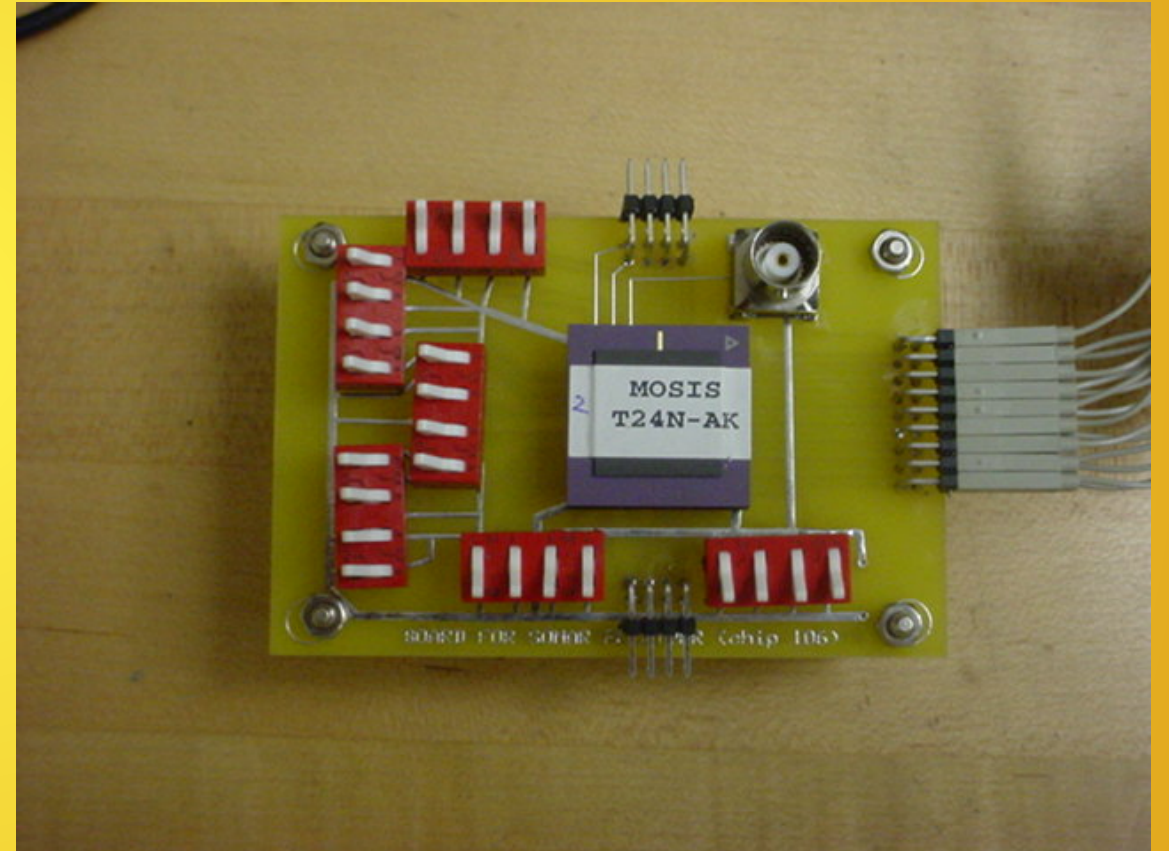
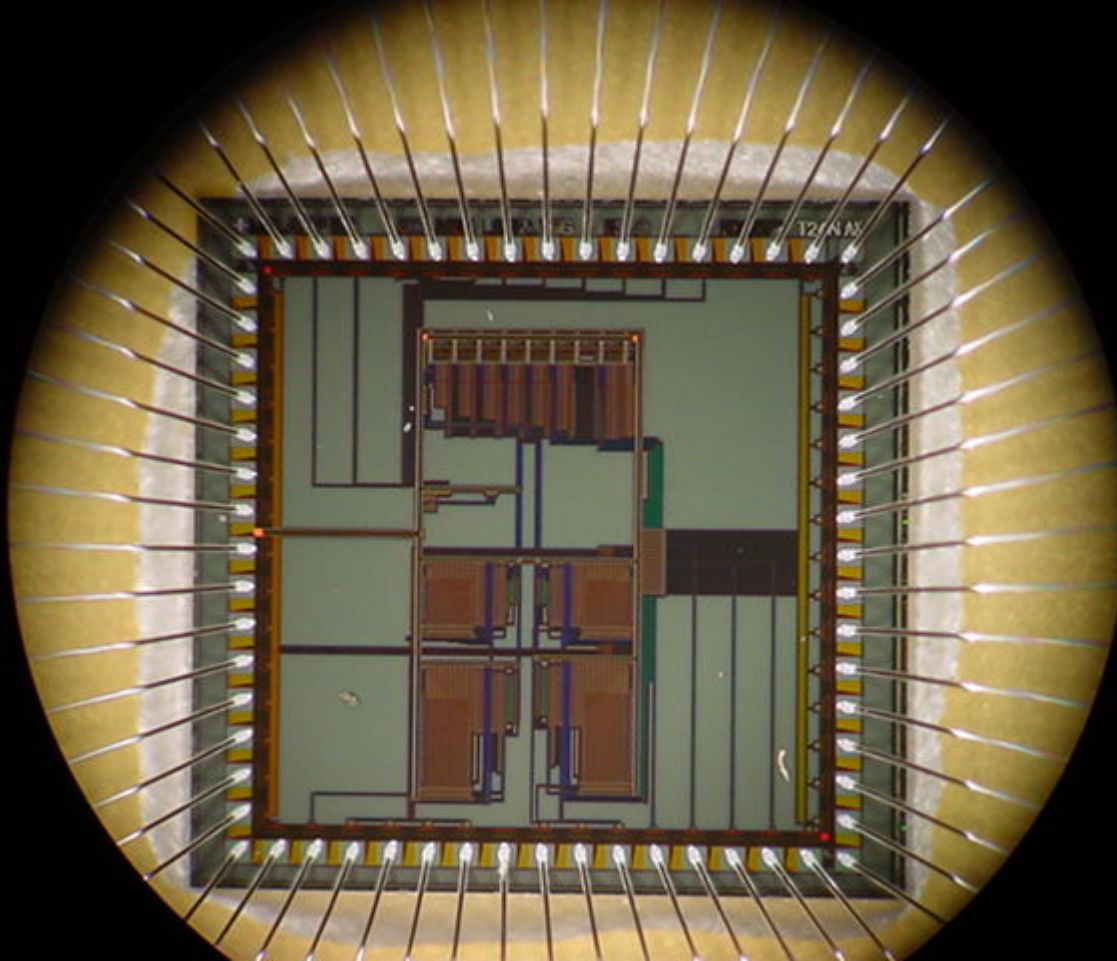
Layers Panel:

| Layer | Purpose | V | S |
|---------|---------|-------------------------------------|-------------------------------------|
| nwell | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| nactive | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| pacive | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| nselect | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| pselect | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| poly | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| metal1 | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| metal2 | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| cc | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| via | drawing | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |

Objects Panel:

| Object | V | S |
|----------------|-------------------------------------|-------------------------------------|
| Shapes | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| Circle/Elli... | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| Donut | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
| Label | <input checked="" type="checkbox"/> | <input checked="" type="checkbox"/> |
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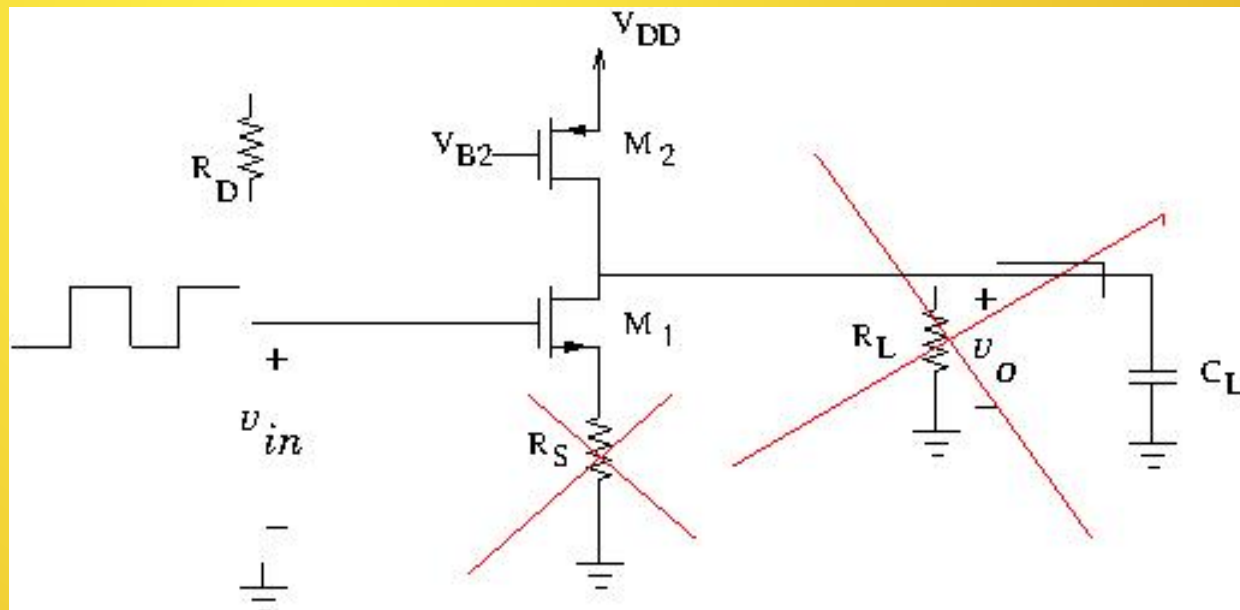
ICs Testing



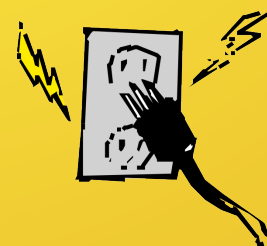
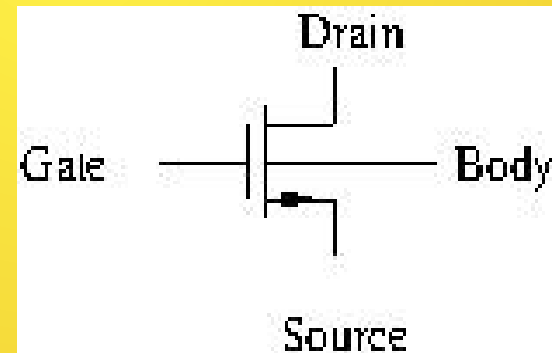
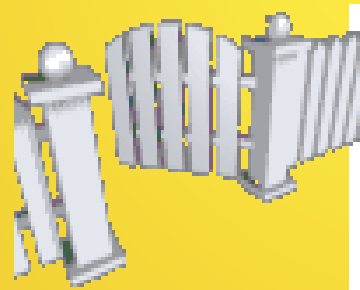
Use Pseudo nMOS & CMOS Inverters to Introduce Static Logic Families

Electronics I (Linear Circuits, Current Source Models & Resistors) Digital Integrated Circuit Design (Switch Models & Capacitive Loads)

- M2 is a Resistor or Current Source (Active)
- M1 is a Switch (Predominant Model)
- The Switch Output Can: Pull Up or Pull Down to either supply rail (or close to it)
- Binary Switch States: ON/OFF
- Standard Analysis: RC Transient
- Transistor \rightarrow Resistor + Switch
- Inputs/Outputs are Pulses, Not Sine Waves
- 'Stability & Linearity' are traded for fast state changes ($V_{DD} \rightarrow Gnd$; $Gnd \rightarrow V_{DD}$)



We Will Need to Think More About Device Physics/Models (vs Electronics)



URI Cad Tool Environment

Supporting IC Design Courses & Research

We will Need to Effectively use IC Design Tools

- Cadence
 - Virtuoso Schematic & Symbol Editor
 - Virtuoso Layout Editor
 - Analog Design Environment (ADE)
 - Spectre
 - Dracula, Assura & PVS: Design Rule Check (DRC) & Layout Vs. Schematic (LVS)
- Mentor Graphics
 - Calibre (DRC & LVS)
- Synopsys
 - Hspice
 - Cscope
 - TCAD Sentarus

Topics

- Switch Models for MOS Transistor Analysis/Synthesis
- RC Models/Transient Response for Timing Analysis
- Understanding Device Physics → Designer's Point of View
- Device Technology Scaling and its Implications on a Designer
- Synthesis of Basic Gates to Building Blocks (e.g. Adders, Mux's, etc.) to Systems
To an Entire IC
- Detailed Study/Analysis of High-Speed Cells (usually one type/family)
- Overview of Highlighted System/Project
- Logic Families: Static CMOS, Pseudo nMOS, Dynamic Logic
- Circuit Simulation Tools → HSPICE and Spectre
- Design Flow → Cadence/Mentor Graphics
- Layout
- Verification
- Manufacturability, Reliability, Yield

Summary

- Our *Space* is Delivering a Layout with working circuitry → layout → reticle mask
- The *objective* is to understand the custom IC design process using automated CAD tools
- The Project Based Course: Grading will be based on: Labs, Hwk, Assignments and a Final Design Project
- Students will learn about the influence of device Physics on MOS transistors realized with smaller geometries (including non-ideal effects) from a *designer's point of view*
- Students are expected to understand basic circuit analysis, Emag(PH204) and Electronics I (ELE212/215; ELE 338/339)
- A basic understanding of digital logic, e.g. gates, latches, flip-flops, counters, adders, etc. is also required (ELE 201/202)