ELE 539 Design Project

Students can select one of two projects:

1. OTA

Provide a layout of the folded cascode OTA, ota_fc_pchin_tsmc180, the current source, bias_CMp2_tsmc180, and the beta multiplier, biasRef_beta_tsmc180. You should copy these cells from the library.

You will need to apply analog layout techniques. An overview is provided in section 18.2, pp 635-644. In designs like this one, the most critical part of the layout will be the diff pair. You will need a common centroid layout, described in figure 18.19 on pp. 641. This is referred to as an interdigitated layout. If the diff pair is realized via transistor M1 and M2, then each specific transistor, M1 and M2, are realized via multiple transistors. The idea is shown below:

M1-M2
M2-M1

To further refine the layout:

D-M1-M2-D
D-M2-M1-D

where D are dummy transistors.

Start with the folded cascode amplifier. This will have a p-channel diff pair. Then work outwards towards the transistors for the tail current source; also the common gate transistor + the bias transistors around it.

The beta multiplier also has a simple diff pair (n-channel) which should have a similar layout.

Prepare the amplifier layout;

- layout the OTA; verify that it passes drc checks and lvs checks
- layout the beta multiplifer + the current mirror.
- propose possible changes to improve slewing (the slew rate) beyond what the current fc OTA can provide (no layout is required; perhaps a simulation or an analytical argument).

2. 1-bit 3$^{rd}$ order sigma-delta modulator.

Design a 3$^{rd}$ order sigma-delta modulator. This modulator should have the following specifications:

- OSR=64
- fs=10MHz
- use the delay pattern outlined in the sample delsi file (for the 5$^{th}$ order modulator), iflf5d.m
- the maximum amplitude of the input signal should be Vref/2.

Once the design coefficients are generated; then you will need to implement a schematic level sigma delta ADC.

C_1_in = 1pF; C_2_in = C_3_in = 500 fF. C_delta = C_1_u*r/(g_2*g_3)