Home Work Assignment #1

Analog Integrated Circuit Design

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Parameters, Equations:

Physical Constants:

$q = 1.6x10^{-19}C$	$\epsilon_o = 8.85x10^{-14}F/cm$
$\epsilon_{ox} = 3.9\epsilon_o = 3.45x10^{-13}F/cm$	$\epsilon_{Si} = 11.7\epsilon_o = 1.04x10^{-12}F/cm$
$n_i = 1.45x10^{10}cm^{-3}$	$\phi_T = 26mV$

AMI C5 Process Parameters:

$CGDO = CGSO \approx .2fF$	$t_{ox} = 13.9nm$
nMOS	pMOS
μ_n=$453cm^2/[V-sec]$	μ_p=$201cm^2/[V-sec]$
V_{Tn}=0.669 V	$V_{Tp} = -0.915V$
$C_{j-sw} = 0.34fF/\mu m$	$C_{j-sw} = 0.23fF/\mu m$
$C_{j-A} = 0.41fF/\mu m^2$	$C_{j-A} = 0.64fF/\mu m^2$

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1) Find the expressions to estimate the pole frequencies, f_{p1} & f_{p2} and the zero frequency, f_z, for the common source amplifier shown in figure 1. Include the voltage source resistance, R_S, in the expressions derived for each frequency as shown in figure 2.
   a) Show that

   $\mathrm{f}_{p1} \approx \left(\frac{1}{2\pi}\right) \frac{1}{g_{m1}C_{gd1}R_s(r_{o1}||R_{oP})}$
   &
   $f_{p2} \approx \left(\frac{1}{2\pi}\right) \frac{g_{m1}C_{gd1}}{C_{gd1}C_{gs1}+C_o\left(C_{gd1}+C_{gs1}\right)}$

   b) Find an expression for R_{op}.

   c) Assuming that we concern ourselves only with gate-source and gate-drain capacitances, which capacitor is C_o (in M2) ?

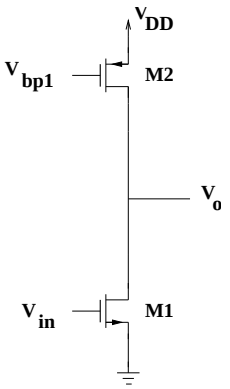

Figure 1. nMOS Common source with active pMOS load.

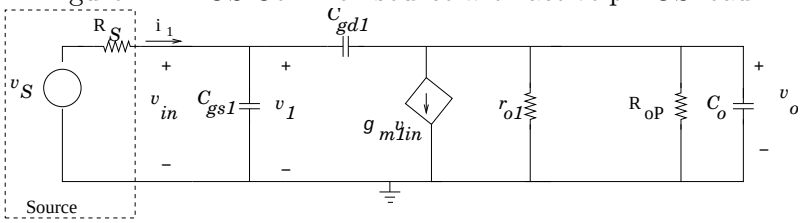

Figure 2. Small signal Equivalent Circuit.

2) Simulate the circuits in figures 1 and 2.

   a) Determine I_D directly from the simulation for your values of W_n, W_p & L.

   b) Compute C_{ox}, k_n, β_n, k_p, & β_p using the values provided (and your device geometries).

   c) Estimate the values of C_{gs1}, C_{gd1} & C_o.
   note: gate drain capacitance (for M1 in saturation) is computed from
   $C_{gd1} \approx C_{ox} W_n L_{diff} = CGDO \times W_n$
   where $CGDO$, is spice parameter for the gate-drain overlap capacitance, defined as $CGDO = C_{ox} L_{diff}$ and L_{diff} is lateral diffusion (the amount of the implant that diffuses under the gate).

   d) Plot the gain and phase of the amplifier using the ac analysis.

   e) Draw the small signal equivalent circuit schematic (in the virtuoso schematic editor); use vccs and assign the g_{m1} value to it. Run the ac analysis for this circuit.

   f) Compute f_{p1}; compare the computed value with each of the ac simulation plots in ADE.

3) Find an approximate expression for f_{p1} for the cascode amplifier shown in figure 3.

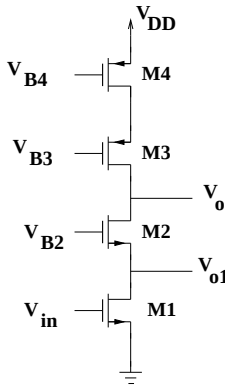

Figure 3. Telescopic Cascode Amplifier with an active load.

a) Draw the small signal equivalent circuit. (*Please note that the pMOS cascode section can be replaced with a resistor,* R_{oP}).

b) Find an expression for the mid-frequency input impedance of the common gate transistor (M2); ignore the body effect (e.g. do not include g_{mb}).

c) Find expressions for the mid-frequency amplifier gain, $\left(\frac{V_{o1}}{V_{in}}\right)$ & $\left(\frac{V_o}{V_{o1}}\right)$; use these expressions to find: $\left(\frac{V_o}{V_{in}}\right)$.

d) Use Miller's Theorem to compare the dominant pole frequency, f_{p1}, of the telescopic cascode amplifier with that of the common source amplifier.