ELE447 Digital Integrated Circuit Design I

Syllabus Spring 2017

Instructor: Dr. A. J. Davis davis@ele.uri.edu
Kirk 204
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Office Hours: TBA.

Lecture: Friday; 5:00-7:45pm Pastore 350

Credits: 3

Pre-requisite: ELE 338, ELE339, PH204, ELE212, ELE215 and concurrent enrollment in ELE448, Digital Integrated Circuit Design I Lab.

Text: D. A. Hodges, H. G. Jackson, R. A. Saleh, *Analysis and Design of Integrated Circuits*, 3rd edition, McGraw-Hill, 2004. ISBN 0-07-228365-3.

A. J. Davis, *Introduction to Integrated Circuit Design, Layout & Simulation*, Laboratory Manual, 2004.

Other sources of information provided on line.

Objective: Develop expertise in digital integrated circuit design; employ custom analog transistor circuit design and MOS Device Physics to realize basic cells.

Topics

CMOS Logic, Switch Models & Simple RC Models
IC Fabrication, Layout & Design Rules
Device Physics, MOS Models, Device Scaling & Short-channel effects
Inverters (CMOS, Pseudo NMOS)
Static CMOS & Pseudo NMOS Logic Gates
Pass Transistor Logic
Dynamic Logic & Other CMOS Logic Families
Timing Clock Routing
Buffers, Pad-Frames
Static/Dynamic Flip-Flops, Registers, Semiconductor Memory, Counters & Arithmetic Elements
CMOS Logic Families/Dynamic Logic
Design Flow
Synthesis/Tools: Cadence Virtuoso Schematic & Layout Editor
Verification/Tools: Synopsys HSPICE, Cadence Analog Design Environment (ADE)
Basic Economics for Full and Semi Custom Approaches

Grading Elements: In order to receive a passing grade in ELE447 students must have a passing grade in each element.

Element	**Weight**
EXAM s 1 & 2	35%
Final Exam	30%
Assignments	20%
Design Project	15%